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IMP D&E (AIMP) PFM ENCODING SYSTEM INTERFACE DOCUMENT

REVISION A

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(AIMP)
PFM ENCODING SYSTEM
INTERFACE DOCUMENT

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March 1965
Revision A
August 1966

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

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INTRODUCTION

This description is written in four parts. The largest section is in Part III where each experimenter and instrumenter may consult the table of contents and find his interface. Thus, only a small part of Section III will be of specific importance to each experimenter.

Part I should be of particular interest to the data processing people and to experimenters who have flown experiments on IMP's A, B or C.

Part II is a brief description of the system to be used in IMP's D&E and should at least be scanned by each experimenter to find the portions of importance to his experiment. It is hoped that every experimenter will read Sections E and F.

Part IV describes the DDP and should be read by all digital experimenters.

Those people involved in data processing and systems integration at GSFC should probably read the entire document.

The telemetry encoding system hardware is identical for both AIMP D and AIMP E; however, some changes in terminology reflect changes within the rest of the spacecraft. Note that this document defines two bursts per channel, 16 channels per frame, and sequences 1 through 16. Some AIMP documents use different definitions for channels and sequences.

PART I. DIFFERENCES BETWEEN IMP's D&E AND IMP's A, B & C(*)

The encoding system used in IMP's D&E will be a natural outgrowth of the PFM system used in IMP's A, B & C.

The encoding system will still be made of two parts called the Encoder and the Digital Data Processor (DDP).

A list of the most significant changes follows:

1. All sequences are essentially the same (e.g., no fourth Rb sequence).

2. The "blanks" will always be filled with data.

3. An Xtal controlled 16-level oscillator will be used to send 4 bits per "burst" instead of the non-Xtal controlled 8-level oscillator used in IMP's A, B & C for digital data.

4. Each "Digital channel" (old blank plus burst) will telemeter 8 bits of information (4 during the old blank and four during the old burst) instead of the 3 bits per digital channel in IMP's A, B & C.

5. The digital data will be "coherent" in that each half-channel (e.g., old blank or burst) will contain an integral number of cycles that start on a "known" phase with respect to the satellite clock. There will be 17 possible such frequencies, 16 representing the 4 bits in the sexadecimal "burst" and 1 representing the distinct sync tone.

6. The storage available to the experimenters in the DDP as accumulator bits has been increased to 188 bits (from 105 in IMP's A, B & C).

7. An "S-T" type accumulator (signal or time) has been added to take care of overflow. This accumulator will count pulses up to a maximum and will then count clock pulses for the rest of the accumulation period. Thus, either count (S) or counting rate (T) will be telemetered. (See Section IV.)

8. An attempt will be made to tailor the speed versus power characteristics of each accumulator. The maximum possible rate is still 500 KC but if the experiment can never get to this rate, the input stages of the accumulator will be designed for the lower maximum possible rate.

*See "IMP PFM ENCODER (S-74)" Revision A, August 6, 1962, H. D. White.

9. Xtal controlled clock pulses may be supplied to the experimenters at a maximum rate of 102.4 KC and at a minimum rate of one every 512 sequences. Any clock pulse between these ranges, that is $102.4\,KC/2^{n}$, may be supplied. (Note: the usual sync pulses will also be supplied at the experimenter's request.)

10. The basic accumulator word has been extended to 32 bits (from 15 bits) or 4 channels. Each 32 bit accumulator may be broken up into as many as 4 accumulators where the number of bits in each of the 4 accumulators is divisible by 2.

    a. Each 32 bit group of accumulators is frozen during its readout (e.g., for 4 channels).

    b. Each 32 bit group of accumulators has two options for reset.

        1. The entire 32 bits are reset after readout, or

        2. None of the 32 bits are reset after readout.

"S-T" type and "S" type accumulators may be in the same 32 bit word, for example accumulator 4 may be broken up as follows:

4a = 16 bit "S" type

4b = 16 bit "S-T" type

11. Bit Rate $\cong$ 28.6 bits/seq

Dig Bits/Seq	= 15ch x 11fr x 8 bits/ch	= 1320
Analog Bits/Seq	= 15ch x 5fr x 13 bits*/ch	= 975
Sync Bits/Seq	= 16ch x 8 bits/ch	$\cong$ 128
Total Bits/Seq	$\cong$	2423

*Assume 6½ bits/analog data burst (i.e., 1% data) Bit Rate $\cong \frac{2423 \text{ bits/seq}}{81.82 \text{ sec/seq}} \cong$ 29.6 bits/sec.

PART II. DESCRIPTION OF IMP D&E ENCODING SYSTEM

A. GENERAL

The telemetry system used in IMP D&E is one of the latest of a series of PFM (Pulse Frequency Modulation) satellite encoders that started with Vanguard III.

It is a direct outgrowth of that used in IMP's A, B & C. (See Section I for a list of the main differences.)

Figure 1 illustrates the basic system. The encoding system accepts three basic types of inputs as follows:

1. Outputs from analog experiments in the range of 0 to +5 V DC.

2. Outputs from experiments requiring pulse accumulation. Pulses are accumulated in "S" type accumulators (straight binary counters) or "S-T" type accumulators (straight binary counters unless overflow occurs; if overflow occurs the accumulator counts clock pulses thus giving the time, "T", required to accumulate the maximum number of pulses). The information is stored in the accumulators until readout time, when their outputs are electronically commutated, 4 bits at a time, into a series of adjacent sexadecimal bursts. Thus a 32-bit accumulator would be readout in 8 adjacent bursts of 4 channels. Each accumulator is readout in this manner. The accumulators are "frozen" during readout (will not accept pulses) and may be reset immediately after readout. (See Section IV.)

3. Digital outputs from digital experiments that are not amenable to accumulation. The encoder supplies a shift signal to the experiment and electronically commutates the information on 4 wires into a sexadecimal burst. The experiment shifting must be completed within 100 microseconds after the initiation of the shift signal. The state of the 4 experiment bits must not change during the .160 second burst. This scheme is recommended instead of scanning to save wires and experiment bits should be arranged, in such a manner, that minimum bit reordering is required in the computer. (See Page 10.)

The pulse frequency bursts are derived from an analog oscillator or a single 17 level Xtal controlled "digital oscillator" (frequency synthesizer).

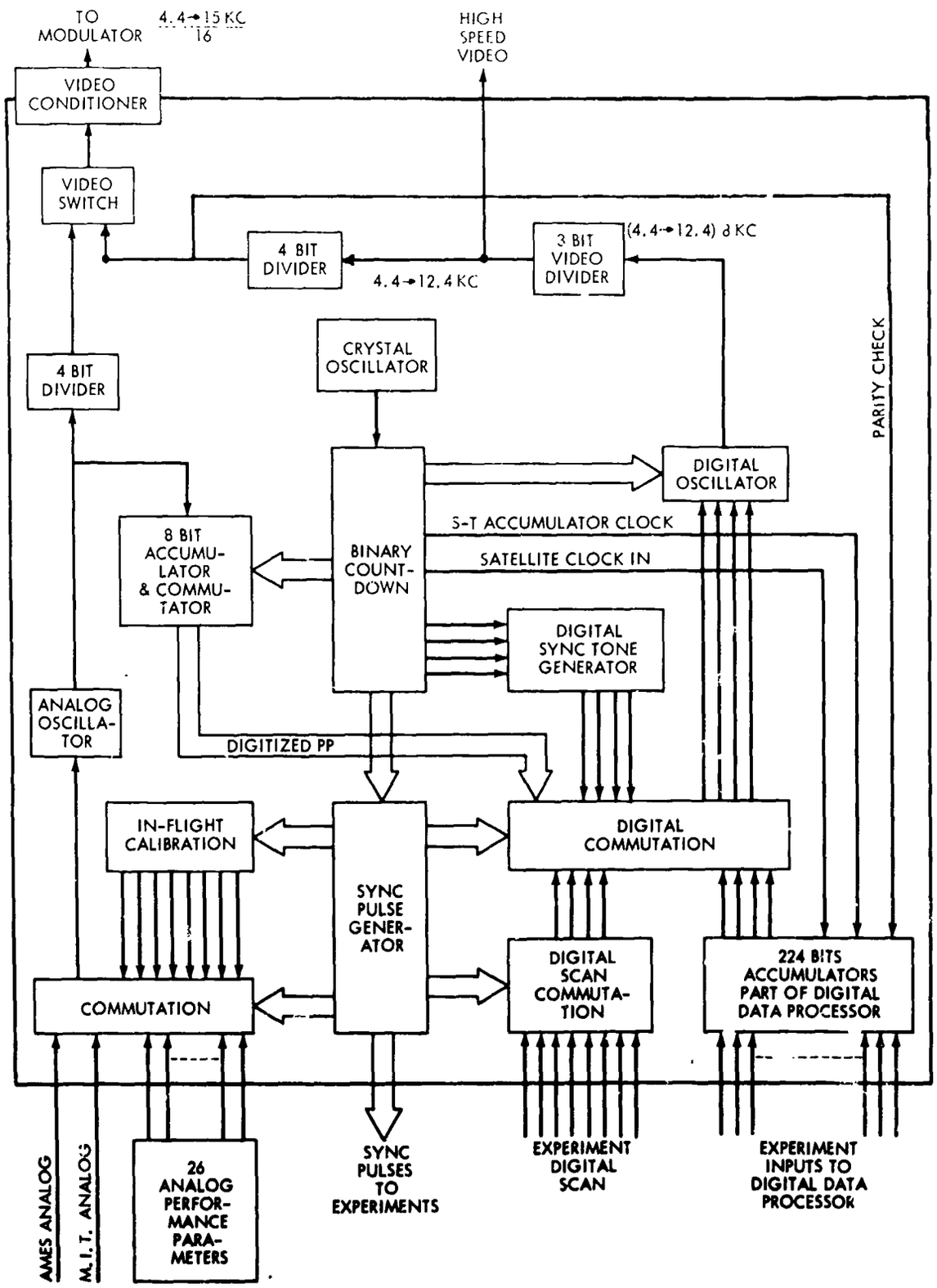


Figure II-1. IMP D & E Block Diagram

Sixteen levels are analogous to the 16 possible combinations of four bits and the 17th level is a discrete tone burst used for synchronizing the data processing equipment. The output of the "digital oscillator" is in the range of (4.4 to 12.4 KC) x 8. A delay is introduced to an accumulator which counts down the burst by 7 binary stages to give the video output in the (4.4 to 12. KC) ÷16 range. This 7 bit countdown is reset after each burst (0.160 seconds) and since each of the 17 possible frequencies contain an integral number of cycles in the burst time, the digital data video out is coherent to a useful accuracy.

The digital data will be synthesized as defined in Figure II-2.

The burst frequency contains the intelligence contained in the state of four binary bits or that of an analog sample. The location of the burst in the telemetry sequence identified the parameters being measured. (See page 7.)

The timing for the system is obtained by counting down a 409.6 KC Xtal controlled clock frequency in a string of 24 binaries (called a countdown unit). The states of the binary counters in the countdown unit are then sampled by appropriate logical circuit elements in a matrix to produce the required commutation gating pulses and synchronizing pulses.

B. TELEMETRY FORMAT AND DATA PROCESSING INFORMATION

The telemetry format is shown in Figure II-3. Since PFM is a time division multiplex, the basic format is arranged as 256 channels with 16 channels in a frame and 16 frames in a sequence. The 16 channels in a frame are labeled 0 through 15. The 16 frames in a sequence are labeled 0 through 15. This nomenclature is a holdover from previous PFM systems where a "channel" consisted of a blank followed by a burst. Thus, each channel was a sample. In IMP D&E, the "blanks" are now filled in with data so that a channel now contains 2 bursts. Since the sequence time is 81.92 seconds, the digital bit rate is 25 bits per second. (The total bit rate is slightly higher due to the analog burst-burst data.)

Please note that if the analog tape is sped up by exactly 16, the data will be in the 4.4-to-15 KC range and each channel will be 20 MS long. The A/D line need not acquire "sequence sync" since each sequence may be processed the same. All the data may be processed as "comb filter date," allowing the computer to convert all digital data to sexadecimal numbers.

Channel zero of each frame, which contains frame identification sends its information for the entire channel time of .320 seconds.

The digital data will be synthesized as defined below:

Sexadecimal Level	Frequency - Cycles	Input Bit Configuration IV III II I
15	6.4 KC/16 = 400	1111
14 (FRO I.D)	6.8/16 = 425	1110
13	7.2/16 = 450	1101
12 (FR2 I.D)	7.6/16 = 475	1100
11	8.0/16 = 500	1011
10 (FR4 I.D)	8.4/16 = 525	1010
9	8.8/16 = 550	1001
8 FR6 I.D)	9.2/16 = 575	1000
7	9.6/16 = 600	0111
6 (FR8 I.D)	10.0/16 = 625	0110
5	10.4/16 = 650	0101
4 (FR10 I.D)	10.8/16 = 675	0100
3	11.2/16 = 700	0011
2 (FR12 I.D)	11.6/16 = 725	0010
1	12.0/16 = 750	0001
0 (FR14 I.D)	12.4/16 = 775	0000

Sync Oscillator 4.4 KC/16 = 275
Where 0 = -5 V to +0.25 V
1 = >+3 V <+7 V
and most sig. bit is IV

Expected tolerance + 0.2%, - 0.1%
Extreme freq. limits ± 1.0%
Expected stability better than .01%

Figure II-2

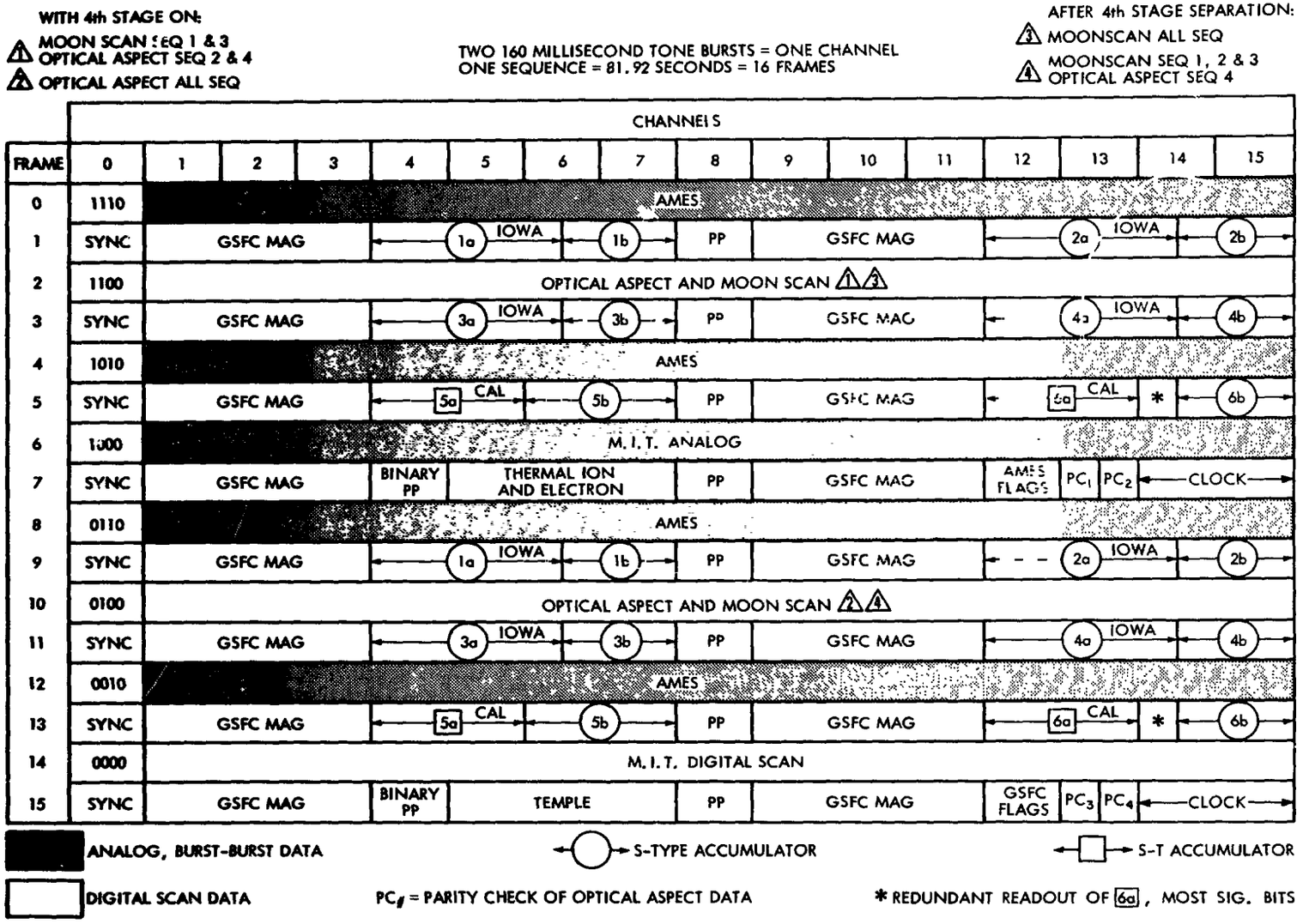


Figure II-3a. IMP D Format

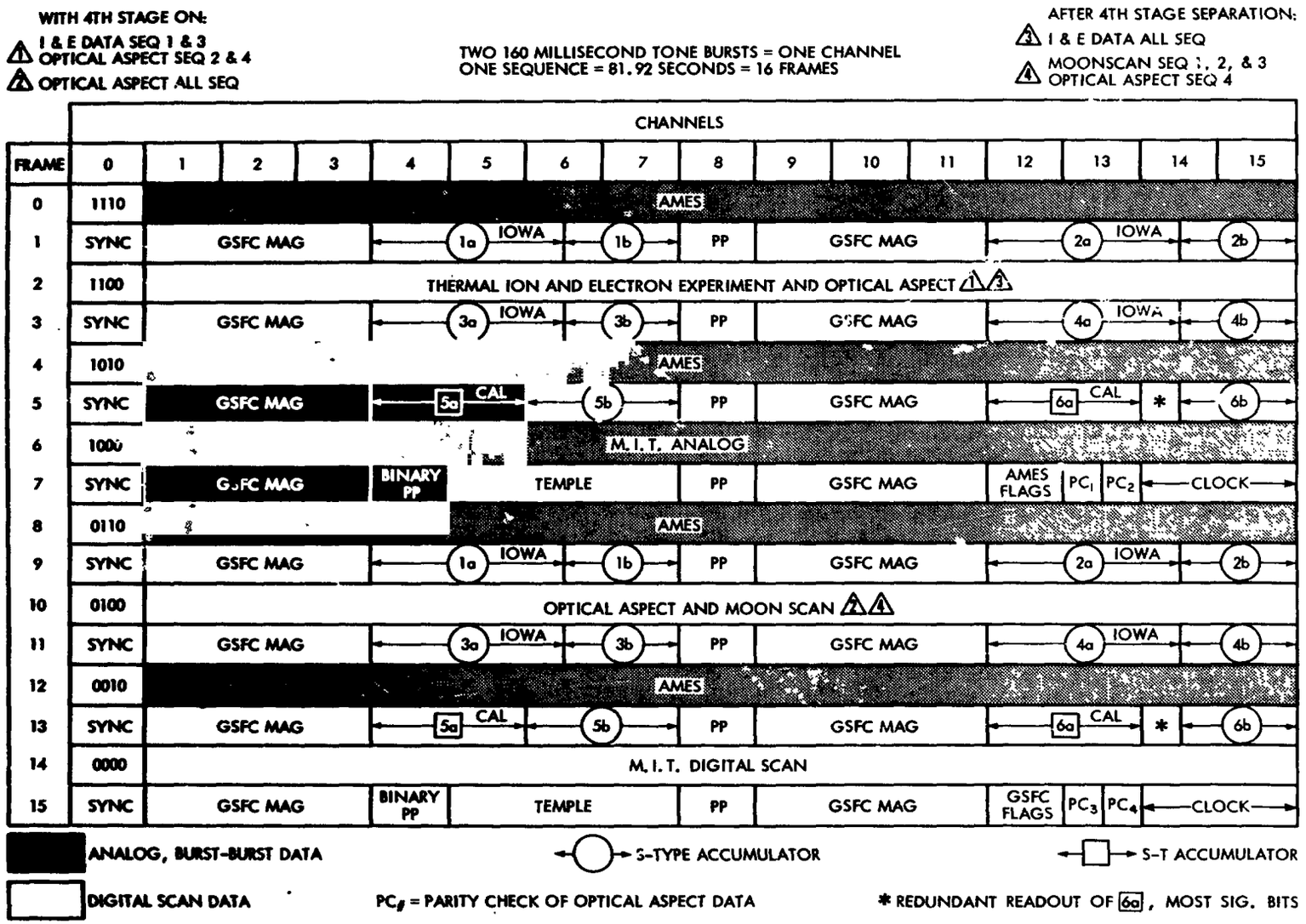


Figure II-3b. IMP E Format

IMP's D&E, as in previous IMP's, contains a sequence counter ("satellite clock") that will have a capacity of 60 days. This clock, of course, may be used by the computer, in conjunction with optical aspect data, to resolve timing problems. The clock may be put to many other uses by programming techniques.

C. READOUT OF EXPERIMENT DIGITAL WORDS

Some digital experiments are not amenable to accumulation and must be readout into the telemetry. Various methods have been used in the past to accomplish the readout. Since the number of bits per channel has increased from 3 to 8, the number of wires required for some readout techniques will become prohibitive since the encoding system packing density is becoming connector-bound. All methods have disadvantages and advantages and each experiment will be treated on an experiment-by-experiment basis.

Four methods will be discussed assuming 32 bits are required for readout.

1. Method I "Direct Scan"

In this method, very commonly used in the past, a wire is received from each bit and directly scanned in the encoder. Thus, 32 wires are required for 32 bits, which is the main disadvantage of the direct scan method. The advantages of the method are that the experimenter needs no complicated matrix or shift register in his package although he must work with a negative four-or-five-volt supply to obtain the best system performance. Another advantage is that the readout is directly slaved to the encoder clock and countdown, and thus there is no chance of "slipping bits". A further advantage is that the bits are scanned in order.

2. Method II "Indirect Scan" (See Figure II-4.)

In this method the wires are reduced from 32 to 12 for 32 bits. This method has also been used in the past with excellent success (Optical Aspect in IMP's A, B & C.) The main advantage of this system over the direct scan method is the saving of wires. The readout is also slaved to the encoder. The disadvantage over Method I, from the experimenter point of view, is that he must do the "anding" of his bits with the encoder supplied sync pulses four bits at a time into the encoder. The encoder sync pulses are negative when the four bits associated with it are to be readout and positive at all other times. In addition each sync pulse sometimes must be conditioned by the experimenter.

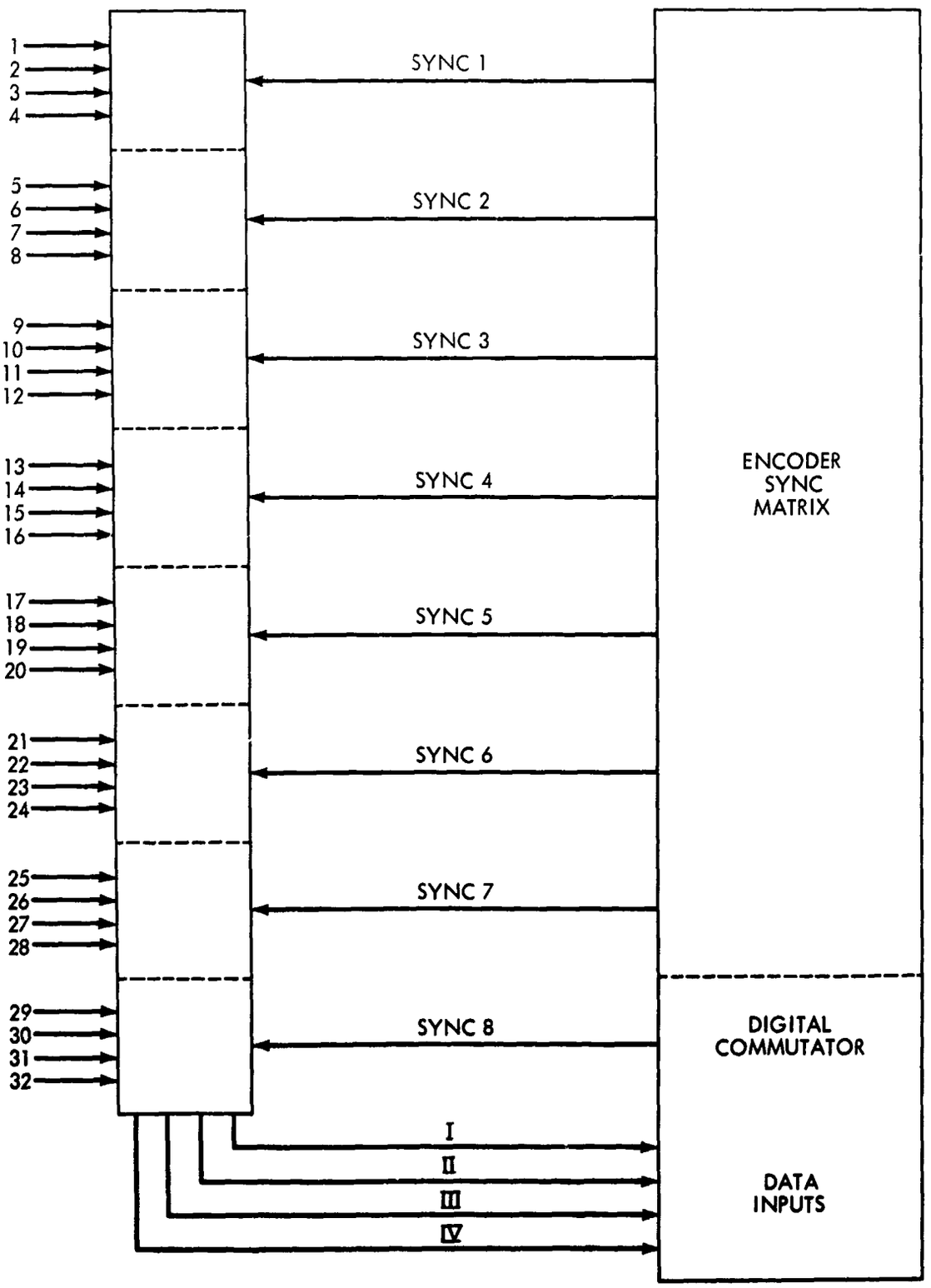


Figure II-4. Indirect Scan Method (Readout Method II)

Another advantage of this method is that the bits are scanned in order and that the experimenter need not have a shift register.

The sync pulse generation for the indirect scan is more complicated than those required for the direct scan; therefore, the total electronics required for the indirect scan is generally more complicated than for the direct scan.

3. Method III "Countdown Reconstruction" (See Figure II-5.)

In this method the encoder supplies the experiment the channel rate, called $\bar{S}$, at the rate of 50/16 CPS and the sequence rate, called $\bar{A}$, at a rate of 1 cycle every 81.92 seconds. The experimenter then drives an 8 binary stage in his package with $\bar{S}$ and resets them once/sequence with $\bar{A}$ to get his binaries (called H' through A') in phase with the encoder countdown. Once the countdown is reconstructed, the experiment can generate any required pulse to scan his word four bits at a time into the encoder on just four wires. This method saves wires in that only 6 interface wires are required for any number of bits. The main disadvantage is that the possibility exists that a failure could cause the experiment countdown to get out of phase with the encoder countdown, resulting in garbled data.

This method becomes very attractive if the experiment requires much commutation of internal electronics in addition to the readout problem. In this case, the encoder would have to supply many additional sync pulses in addition to those described in previous methods. With this method, the experimenter then generates all sync pulses in his package and reduces the interface problem and his checkout. In other words, his package is almost self-contained.

Method 3 is not recommended to solve the problem of just reading out experiment digital words but should be considered if many additional switching functions are required by the experiment.

4. Method IV "Shift Signal Method" (See Figure II-6.)

This fourth method causes the experimenter to have a shift register in his package and may be used for any size word. Figure II-6 shows a 32 bit series shift register that is shifted 7 times, one bit at a time, in order to read out the 32 bit word. The first readout, bits 8, 16, 24 and 32, are readout by the encoder before a shift signal is applied. The 8th positive going waveform may cause his register to shift or not, at his discretion, since the encoder will not readout this experiment at this time.

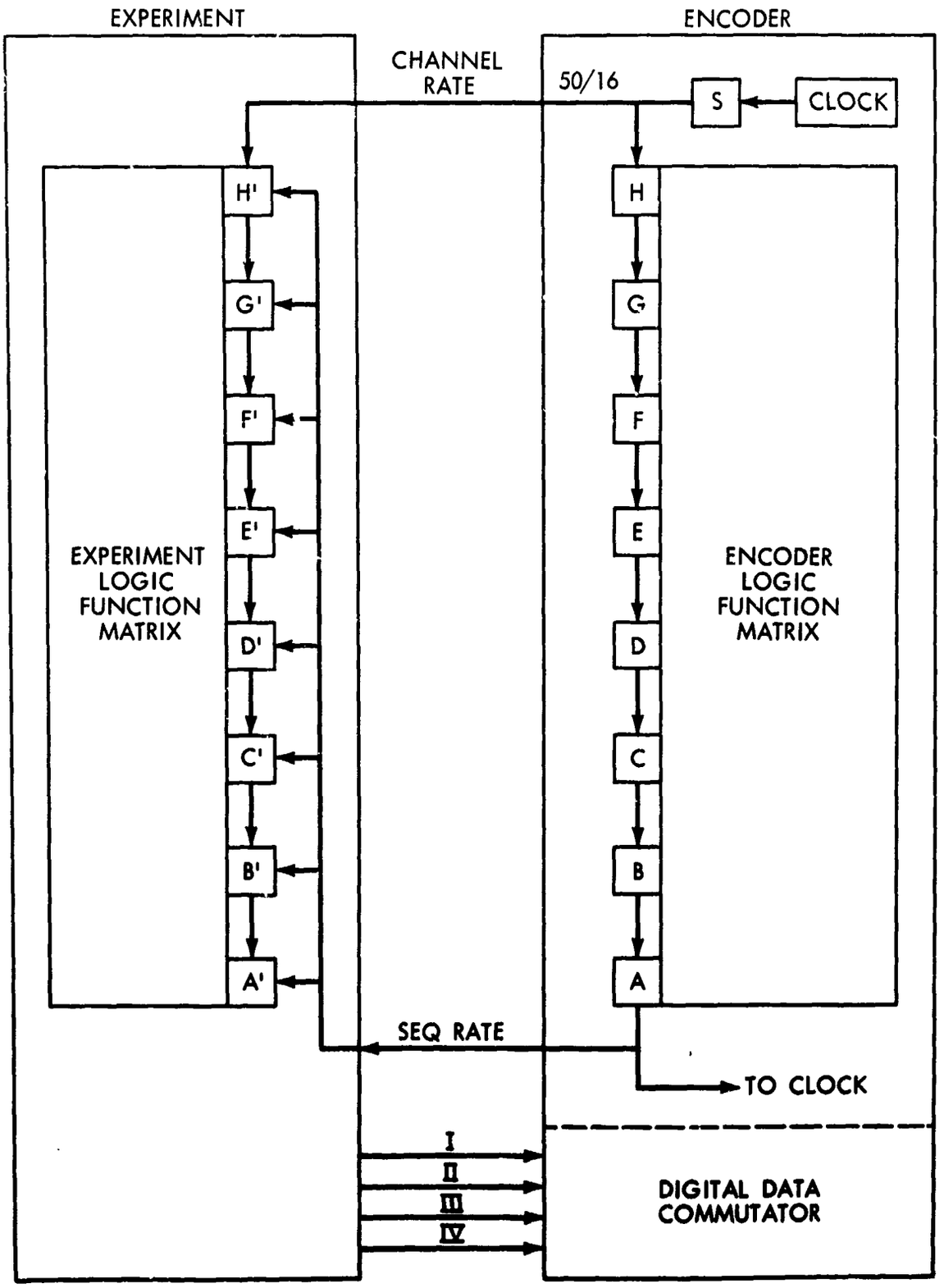
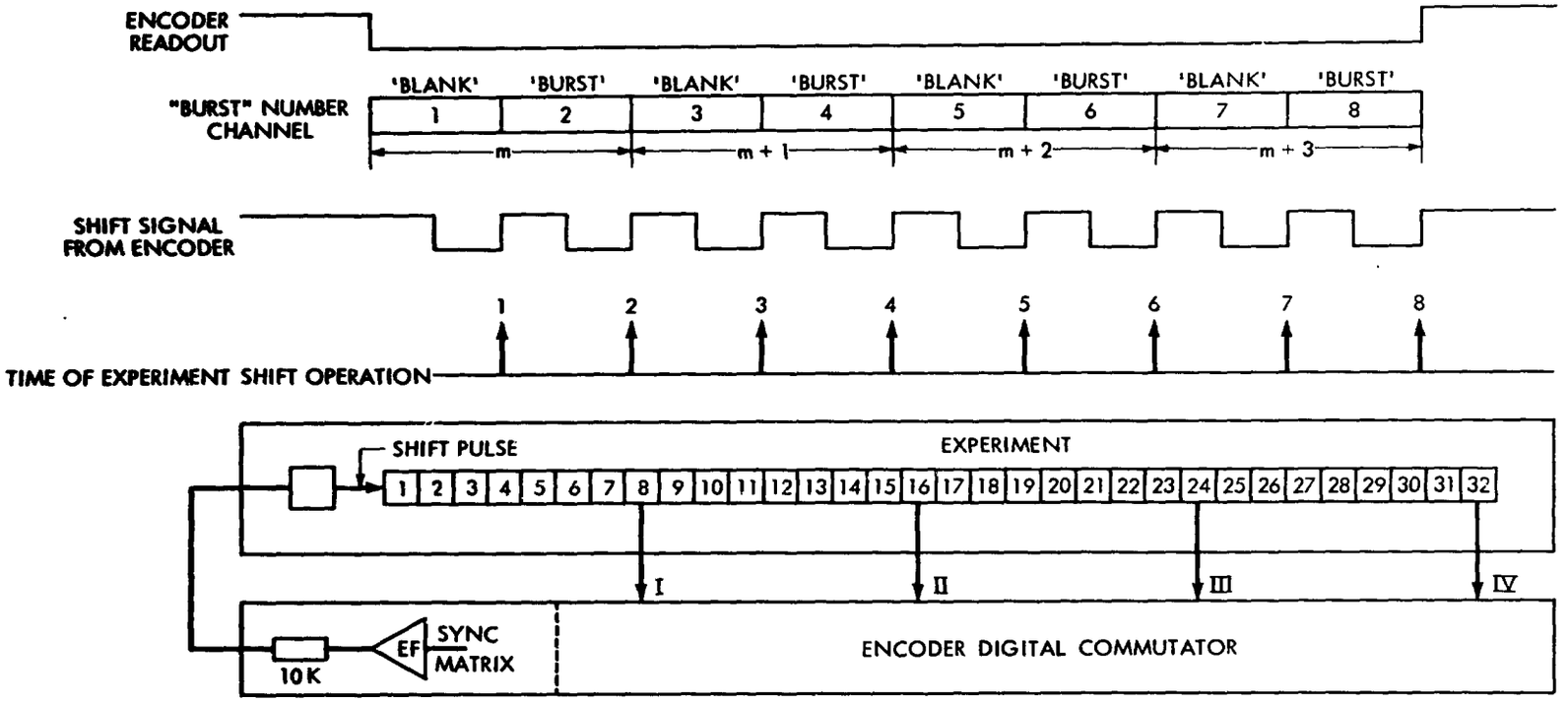


Figure II-5. Countdown Reconstruction Method (Readout Method III)



SHIFT PULSE NUMBER	BIT STRUCTURE				BURST NUMBER OF READOUT
	I	II	III	IV	
NONE	8	16	24	32	1
1	7	15	23	31	2
2	6	14	22	30	3
3	5	13	21	29	4
4	4	12	20	28	5
5	3	11	19	27	6
6	2	10	18	26	7
7	1	9	17	25	8
8	READ OUT OVER				NEXT EXP

SHIFT SIGNAL METHOD
(READOUT METHOD IV)
SHOWN FOR 32 BITS, BUT
CAN BE USED FOR ANY NUMBER

Figure II-6. Shift Signal Method (Readout Method IV)

It is essential that the experimenter understand two timing considerations:

a. His shifting must be complete in less than 100×10^{-6} seconds from the time the positive going shift signal reaches +3 V DC.

b. The shift register must not change state again until the next positive going swing of the shift signal.

These timing limitations are required so that the sexadecimal burst will never change during the readout.

It is realized that modifications of this scheme are possible, i.e., four parallel 8 bit shift registers could be used.

A possible disadvantage of this scheme is that the bits are not scanned in order. It may be possible, however, for the experimenter to arrange his bits so that the sexadecimal readout is a meaningful entity. As previously mentioned, disordered bit structure may cause a checkout and data processing problem.

The shift signal characteristics will be as follows:

a. Output Z approximately 20K ohms, this is an exception to the rule for sync pulses and is required in this case to keep rise times down to a reasonable value for the shifting.

b. When not being readout, the shift signal is approximately +5.5 V DC.

c. During readout the shift signal will be an approximate square wave as shown on Figure II-6 that goes from approximately -2.8 V to approximately +5.5 V. The experimenter is to initiate his shift pulse on the positive going part of the square wave.

d. The shift signal may have noise spikes of duration less than 10×10^{-6} seconds.

This method is attractive for experiments that already have shift registers and requires the least amount of encoder sync pulse generation and wires in the cable. For large words in the experimenter package (greater than 16 bits), this method is suggested.

The disadvantages of the method are numerous, some of which are listed:

a. Experiment may have to use a shift register that would otherwise be unnecessary.

b. Possibility of experiment word getting out of sync with the encoder exists.

c. Possible problem with bit ordering exists.

Timing should not be a problem since 100 microseconds should enable low power shift register to be used.

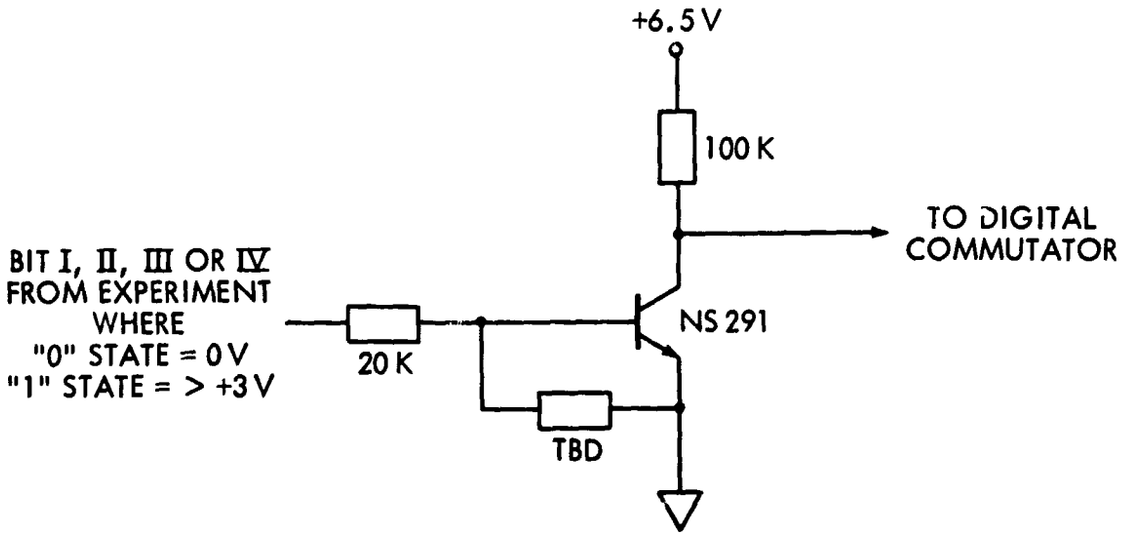


Figure II-7. The Digital Scan Interface Circuit

D. ANALOG DATA

Two experiments will contain analog data. The Ames magnetometer and part os the MIT data will be converted from a 0-to+5 volt signal to a 15 KC-to-5 KC frequency, and then the video will be divided by 16.

The analog performance parameters will be digitized and transmitted as sexadecimal frequencies. There are several advantages to digitization of these parameters.

a. Many of these parameters are needed to make decisions as to when the fourth stage should be fired. The ground support equipment can decode these sexadecimal numbers even in noisy signals, whereas analog data would not be as easily decoded.

b. The matrix defining whether analog or digital data should be decoded is simpler, hence more reliable.

c. The oscillator calibration will be independent of comb filter anomalies, instead of varying due to the filters.

d. The only disadvantage is that the parameters are sampled less frequently, but those infrequently sampled do not change quickly, so no information is lost.

e. Pre-flight checkout can be accomplished much more easily than if the data were telemetered as raw analog.

f. The frames are either all analog or all digital (except for channel 0 sync pulses), thus making the system more standard.

1. Analog Experiment Output Characteristics (except for P.P.)

The analog experiment should vary in the range of 0 V to +5 V full scale and should never exceed +5.5 V when saturated. The experiment voltage output can vary slowly (.05 volts/burst) within the above voltage limits, this dynamic voltage restriction is necessitated by comb filter response.

If the experiment output impedance is less than 1 K ohm, the encoder impedance will have a negligible effect on the number being telemetered, thus the experimenter should be able to match his output voltage versus parameter readings with the encoder input voltage versus telemetered number without taking into account the encoder input impedance.

2. Encoder Input Versus Telemetered Number Characteristics for Performance Parameters

Figure II-8 is the ideal curve of analog input voltage versus decimal conversion of the double sexadecimal channel bursts representing the analog input voltage. Thus, an analog input voltage of 0 V would be changed to 15 KC and converted to the number 219 while an analog input voltage of +5 V would be changed to 5 KC and converted to the number 19. In the referenced curve, the control volt versus number out is linear, so that +2.5 V input voltage will result in a telemetered number 119. The dynamic range of the system is 200 counts for a voltage swing of 5 volts. The counts will be limited by the system characteristics for voltages greater than +5 V DC.

Note Figure II-8 is the theoretically perfect curve and the actual curves will not be this good. Calibration curves will be made of input voltage (at 1 K ohms out) versus telemetered decimal numbers at various temperatures and in-flight calibration will be made. It is hoped that system accuracy of ±1% over the temperature range of 0°C to +40°C will be maintained in this manner.

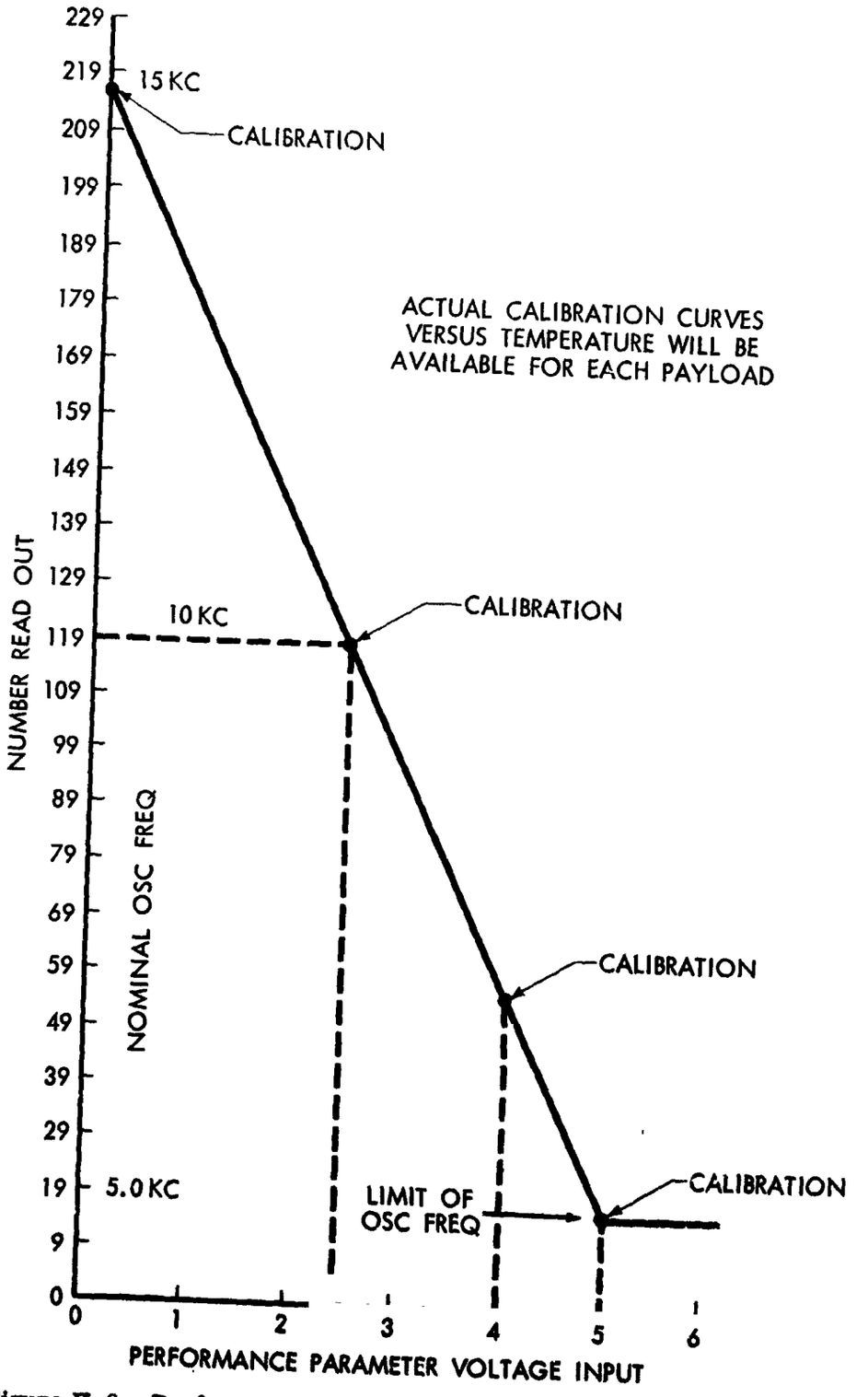


Figure II-8. Performance Parameter Voltage Versus Digital Readout

3. Description of Operation (see Figure II-9)

The two analog experiments and the performance parameters will be commutated into the single analog oscillator. During channel 0,000, a 20 millisecond gating interval allows the pulses generated by the analog oscillator to be accumulated by the 8-bit accumulator. The 8 bits are readout during channel 8 of each odd frame, as one performance parameter. The average of the performance parameter is taken during the 20 MS sample.

Since 15 KC for 20 MS is 300 counts and since 5 KC for 20 MS is 100 counts, the system has a dynamic range (resolution) of 200 counts. It is clear that the 8-bit accumulator will overflow if greater than 256 counts enter it. Thus, it is preset to 175 before the accumulation occurs. This is a strange number, but is chosen because it results in the preset word having the maximum number of "1's" and still being useful. The number 175 was chosen then, to reduce the "race problem" and not for ease of computer usage.

If all works according to plan, with the accumulator preset to 175, exactly 81 additional pulses will cause it to overflow to all "0's". Thus an input frequency of 4.05 KC will result in the number 0 being readout and an input frequency of 12.75 + 4.05 = 16.8 KC will cause the readout number to be 255.

One immediately asks, why not make use of the entire accumulator capacity and have a resolution of 1 part in 256 instead of 1 part in 200? The answer basically is one of hardware, the analog oscillator is tried and proven and is in the 5 to 15 KC range (see reference B) while 20 MS is a 2^n division of the 409.6 KC Xtal, thus 10 KC for 20 MS results in the 200 count dynamic range. Another reason is that it is nice to have some guard bands to insure against overflow in the event of a negative input voltage. The oscillator limits at a frequency slightly below 5 KC (control volts greater than +5 V).

4. Reliability Considerations

One familiar with previous PFM encoding systems will note that this is a very radical departure in that only one analog oscillator is used instead of several (one for each experiment). Indeed, only one digital oscillator is used.

A few of the concepts used in reliability considerations will be listed and a mathematical comparison will be left to the reader if he wishes one.

a. The cross talk problem among analog gates has been resolved by the addition of the SEQ gates. (page 18) This was previously taken care of using multiple "fail safe" OFF analog oscillators.

b. One oscillator takes less parts than more than one oscillator.

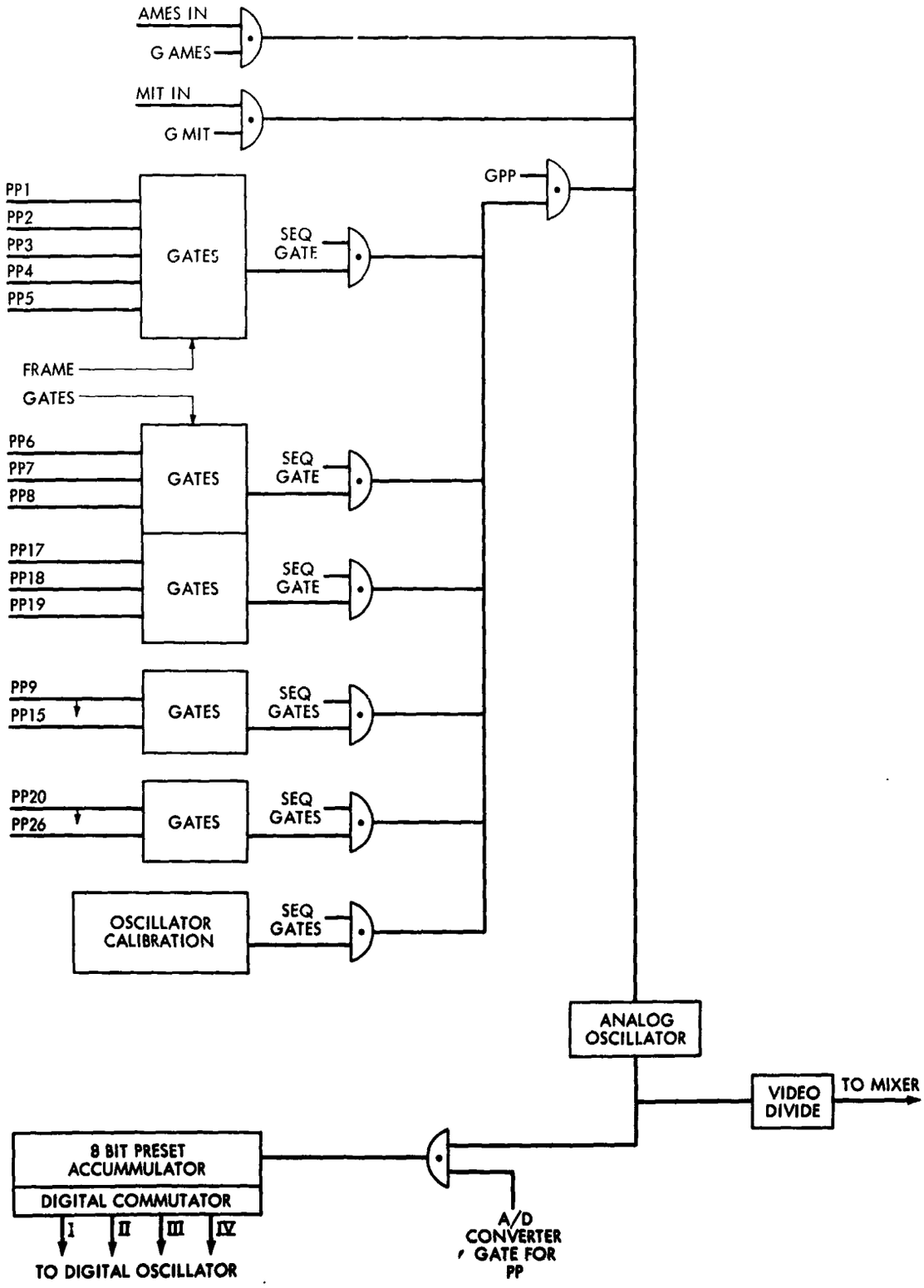


Figure II-9. Analog Data Handling

c. Although the oscillator has been designed with "fail safe" OFF circuitry, multiple oscillators require multiple gating matrices for which a "short" may cause two oscillators to be gated "on" at the same time. This type of failure may be catastrophic with multiple oscillators. In this case, the single oscillator is on for analog data and for 20 MS every odd frame and required gating is done at the accumulator output with a simple NOT digital function.

d. From a systems point of view this single oscillator approach has merit in that in-flight calibration is practical.

5. Analog Oscillator Calibration Procedure

A check of the analog oscillator will be made in-flight, calibration points will be as shown in the following table:

Voltage Source	Readout in Channel 8, Frame 15 Sequence	Purpose
Ground, 0 Volts	2	Check Slope & Bias
Thermistor	4	Temperature
Voltage Standard, 4 Volts	6	Slope and Bias from Absolute Reference
4 Volt Divider	8	Detect 7.5 volt change, slope & bias change & compare with standard
Ground, 0 Volts	10	Check Slope & Bias
Thermistor	12	Temperature
25 Volt Divider	14	Check Linearity
5 Volt Divider	16	Check Knee & Linearity

The data processing people will be given the calibration of the oscillator as determined during encoder burn-in. Comparison of these numbers, with those experienced during spacecraft calibration and flight should be made. Deviations of more than one count indicate a shift in some parameters. The amount of

shift experienced by each calibration point may define the type of parameter shift, and allow data to be corrected to within ±1% of proper value. The addition of an analog calibration flag, based on the correct comparison of all 4 calibration checks (with possible correction due to temperature) should be considered by the data processing people. With consultation of the project staff, correction of analog data in excess of 1% should be found possible.

Table of Oscillator Calibration Capability Showing Minimum Detectable Variations at each Calibration Point, Independent of all others:

Type of Change in Oscillator Circuits	Apparent Voltage Shift (Expressed in Percent of Five Volts Full Scale), Sufficient to Cause a One Count Change at the Accumulator Output.				
	Ground	2.5 Volt Divider	4 Volt Divider	4 Volt Standard	5 Volt Divider
7.5 V Supply Apparent Flux Change (function of Temp)	±0.5% ±0.5%	±0.8% ±0.5%	±1.1% ±0.5%	±0.5% ±0.5%	±1.5% ±0.5%*
Limiter Voltage Nonlinear Curve	0	±0.5%	0	0	-?%** ±0.5%
Slope Changes					
A. About Gnd		±1.0%	±0.6%	±0.6%	±0.5%
B. About +5V	±0.5%	±1.0%	±2.5%	±2.5%	
C. About +2.5V	±1.0%		±1.7%	±1.7%	±1.0%
Shift in 2.5V Divider		±0.5%			
Shift in Standard				±0.5%	

*The +5 V divider reading will be -.5% unless the apparent shift appears to reach the limiter voltage, in which case the % change will be smaller.

**Depends on sharpness of knee of limiter, and if it approaches the 5 volt input.

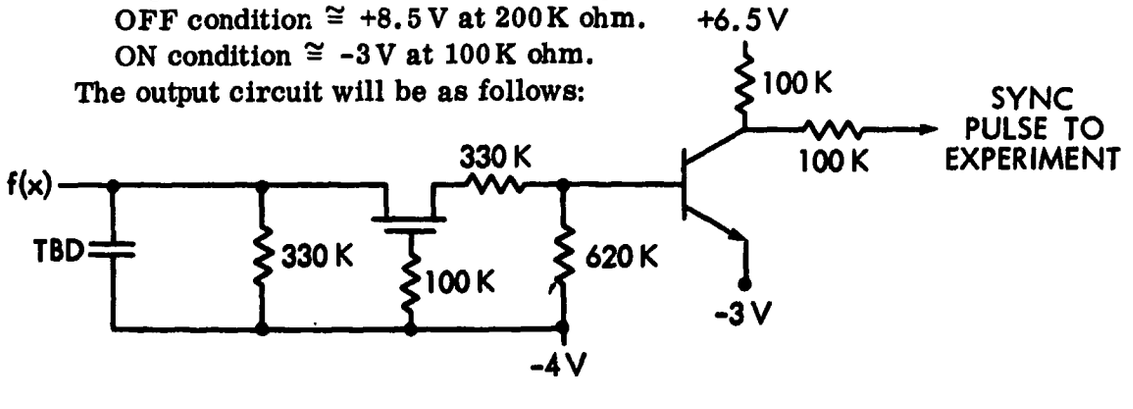
E. SYNC PULSES SUPPLIED TO EXPERIMENTER

No standard sync (timing) pulses are available in a given encoder because the various possible combinations of sync pulses are tremendous. For any given satellite encoder, the experimenter's requirements are analyzed during the initial planning stage and the experimenter requests those pulses he desires. In the case of D&E, the encoding system may become connector-bound, so it is valuable to save wires. (See Section II-C.) Another limitation in IMP's D&E is that of the experimenter no longer having a "blank" time in which to perform his switching since the blank is filled with data. In general, the experimenter has 100×10^{-6} seconds to perform his switching from the time the sync pulse goes to +3 V (if + going) or to -1.8 V (if - going) before any trouble may occur. Experimenters using the DDP may switch during the "freeze" time without causing any problems to the telemetry. The analog experimenters have at least 1 MS in which to switch from the beginning of any channel. Since it is essential that the switching does not cause the PFM burst to change during a channel period, a delay has been introduced into the video divide unit to allow switching times specified above.

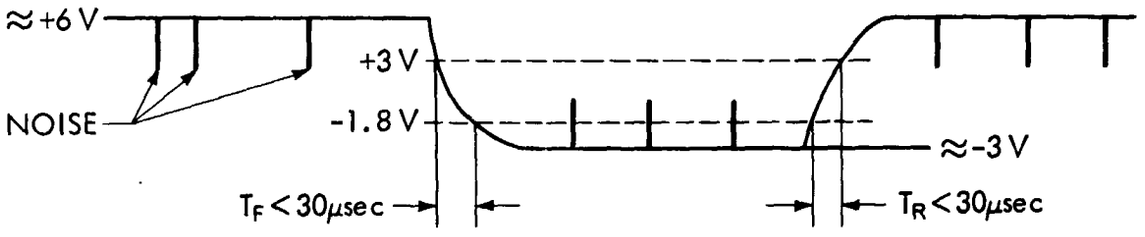
For the most part, any sync pulse can be generated in the encoder so long as it starts at the beginning of any channel (e.g., at the beginning of the old "blank") and ends at the end of any channel. It is obvious that some sync pulses are more easily generated than others so that various trade-offs are sometimes desirable.

All sync pulses, of course, are "timed" or synchronized with the encoder. The main requirement is that the experimenter makes known his requirement before the design freeze date because it is very difficult to make design changes after the encoder is built. Please note that the experimenter should feel free to change his mind about sync pulses up to the design freeze if it simplifies his experiment.

Most pulses have "standard" output inpedances as follows:
OFF condition ≅ +8.5 V at 200 K ohm.
ON condition ≅ -3 V at 100 K ohm.
The output circuit will be as follows:



The rise times of the pulses are very poor.



As shown in the above figure, the rise and fall times are less than 30 microseconds when open circuited at the experiment end.

These pulses have a tendency to be noisy (sharp spikes of a short duration less than 10 microseconds) so that the experimenter receiving these pulses should take advantage of the large voltage swing between the two states to perform his switching. If differentiation of leading or trailing edges of the sync pulse is required, it must be done in the experimenter's package by the experimenter taking into account the noise problem mentioned above.

The Shift Signal has different characteristics. (See Section IIC-4, page 10).

The following table gives basic timing nomenclature.

IMP D ENCODER COUNTDOWN

NAME	FREQUENCY	PERIOD	FORMAT
$4C_1$	409.6 kc	2.44 μs	Clock
$2C_1$	204.8 kc	4.88 μs	
C_1	102.4 kc	9.77 μs	
C_2	51.2 kc	19.5 μs	
C_3	25.6 kc	39.1 μs	
C_4	12.8 kc	78.1 μs	
C_5	6.4 kc	156.0 μs	
C_6	3.2 kc	313.0 μs	
C_7	1.6 kc	625.0 μs	
C_8	800.0 cps	1.25 ms	

continued

IMP D ENCODER COUNTDOWN (continued)

NAME	FREQUENCY	PERIOD	FORMAT
C_9	400.0 cps	2.5 ms	
C_{10}	200.0 cps	5.0 ms	
C_{11}	100.0 cps	10.0 ms	
C_{12}	50.0 cps	20.0 ms	
C_{13} (8S)	25.0 cps	40.0 ms	1/8 Channel
C_{14} (4S)	12.5 cps	80.0 ms	1/4 Channel
C_{15} (2S)	6.25 cps	160.0 ms	1/2 Channel
S	3.13 cps	320.0 ms	1 Channel
H	1.56 cps	640.0 ms	2 Channels
G	781.0 mcps	1.28 seconds	4 Channels
F	391.0 mcps	2.56 seconds	8 Channels
E	195.0 mcps	5.12 seconds	1 Frame (16 Channels)
D	97.7 mcps	10.2 seconds	2 Frames
C	48.8 mcps	20.5 seconds	4 Frames
B	24.4 mcps	41.0 seconds	8 Frames
A	12.2 mcps	81.92 seconds	1 Sequence (16 Frames)
a_1	6.10 mcps	2.73 minutes	2 Sequences
a_2	3.05 mcps	5.46 minutes	4 Sequences
a_3	1.53 mcps	10.9 minutes	8 Sequences
a_4	763.0 µcps	21.8 minutes	16 Sequences
a_5	381.0 µcps	43.7 minutes	32 Sequences
a_6	191.0 µcps	87.4 minutes (1.47 hours)	64 Sequences
a_7	95.4 µcps	2.91 hours	128 Sequences
a_8	47.8 µcps	5.83 hours	256 Sequences
a_9	23.8 µcps	11.7 hours	512 Sequences
a_{10}	11.9 µcps	23.3 hours	1024 Sequences
a_{11}	5.96 µcps	46.6 hours (1.94 days)	2048 Sequences
a_{12}	2.98 µcps	93.2 hours (3.88 days)	4096 Sequences
a_{13}	1.49 µcps	7.77 days (1.11 weeks)	8192 Sequences
a_{14}	745.0 ncps	15.5 days (2.22 weeks)	16384 Sequences
a_{15}	373.0 ncps	31.1 days (4.44 weeks) (1.02 months)	32768 Sequences
a_{16}	186.0 ncps	2.04 months	65536 Sequences

F. CIRCUIT DESIGN AND FABRICATION TECHNIQUES

1. Approaches Taken

The IMP D&E encoding system is functionally much more complex than that of IMP's A, B and C. If a measure of the functional complexity is the number of binary stages required, then IMP D is approximately 2 times as complex as IMP A. IMP A has about 140 binary stages and IMP D has about 250.

IMP A had approximately 5,000 electrical parts, of which 3,000 were not resistors. If IMP D used the same circuit design and fabrication technique it would have approximately 9,400 electrical parts of which 5,600 would not be resistors. None of the above figures include welds. Since the IMP A encoding system pushed the state of the art, using conventional components, it would be very desirable to go some other route with IMP D.

Several approaches have been taken to reduce the IMP's D & E parts count and the main ones are listed:

a. Redesign of electrical circuits (binaries and logic circuits) and improved system design (sexadecimal bursts instead of octal bursts, to make the logic based on a system divisible by 2 instead of 3) in order to reduce the number of parts. This has been done and it is estimated that approximately 2,700 parts can be saved resulting in a "conventional" design with 6,600 parts of which 4,300 are non-resistors. This is still a large number of parts.

b. A monolithic solid circuit approach where two types of low power elements would be used. The elements were a BINARY BLOCK (at 1/2 mw/bit) and a low power LOGIC BLOCK (at approximately 1/10 mw/logic function). The two blocks would be used in approximately 65% of the system and "conventional" components in the rest. Both blocks were based on the improved circuit design above. At this writing, this approach is still in the development stage and does not appear to be feasible for the IMP D & E schedule.

c. The MOSFET (Metal Oxide Silicon Field Effect Transistor) approach. Here again two basic building blocks will be used, a MOSFET BINARY (with resistors added externally). Two promising things happen with this approach, one is that about 93% of the system will be MOSFET blocks or resistors and the other is that the total parts count goes down to less than 4,000 parts where less than 1,000 are non-resistors. Thus, this approach results in about the same number of total parts used in the IMP A encoding system but has even less non-resistor

parts than IMP A. Please note again that IMP D has about two times the functional complexity of IMP A.

In all the above, the assumption is made that resistors are in order of magnitude more reliable than non-resistor (capacitors, diodes, transistors or MOSFET's) parts and may be weighed accordingly in a mathematical reliability analysis.

2. Status of Approaches

a. Conventional Design (using IMP A circuits and logic) is out of the question (about 9,400 parts required).

b. Conventional Design (using simplified binary circuits) is better than the above and will be possible but not desirable (6,600 parts required).

c. Monolithic solid circuit approach for 65% of the system and convention design for the rest is desirable but cannot be used due to schedule problems. (Not feasible due to schedule.)

d. MOSFET approach. Appears to be by far the best from its electrical properties, reduction of parts, and schedule. Its disadvantage is that "SUPPOSEDLY" less is known about its long term reliability than is known about the conventional approach. (Approximately 3,100 parts required where less than 1,000 are non-resistors.)

3. MOSFET Approach Expanded

Since all other approaches except the MOSFET approach are familiar to most readers of this document and since the MOSFET is a new animal, this paragraph is intended to give some of the electrical properties of the device that are useful in IMP encoding system design.

A primary design constraint is power, it must be relatively low. Since we do a great deal of accumulation and storage in the Encoding System Digital Data Processor, binary counters are used. One primary problem then, is how do you make a low power binary, at reasonable speeds (up to 500 KC), that is electrically quiet and that will perform for a year in orbit over the temperature range of -30°C to +60°C. In the past (IMP A) we have used complimentary flip-flops with considerable success. We have developed a 2 transistor "low power" flip-flop to eliminate half the transistors. Either of these devices operate on the principle of using low voltages (supply) and reasonably low resistor values up to about 200 K ohms. The fact that the supply voltages are low implies

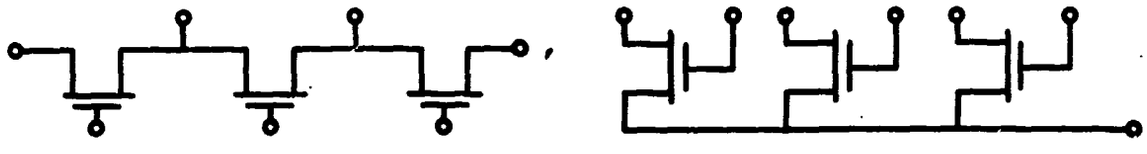
that the "trigger" voltages must be low and this means that the noise rejection threshold is low. The MOSFET binary works on a different principle to achieve low power, it uses large voltages and large resistors. The supply voltages have a difference of potential of 10.5 volts and it takes a "trigger" of about 5 volts (large) to flip them. This gives excellent noise rejection. It should be pointed out here that all capacitors and diodes have been eliminated in the binary design and the device uses a double input threshold level "flipping" technique. Indeed, a binary stage consists of one TO-5 can and four large value resistors where a complimentary flip-flop requires 4 transistors, 6 resistors, 5 capacitors and either 4 or 8 diodes depending on speed requirements. Thus, the low power MOSFET has 5 each discrete parts and the low power complimentary flip-flop has up to 23 parts; this is a parts reduction of better than 4 to 1, and is a "non-resistor" parts reduction of up to 17 to 1!! The fact that the resistors are external enables the designer to obtain an efficient speed versus power profile. Thus, a 0.1 mw low speed MOSFET flip-flop is obtained by using 2 megohm resistors. The external high value resistors used with the MOSFET binary protect against a "short" in a MOSFET binary causing a catastrophic failure by "deadheading" the line. This is particularly important since 80% of the binaries are such that a failure will cause loss of data from only part of a single experiment. The rest of the experiments would still provide useful information.

An especially exciting feature of the MOSFET approach is the elimination of many stages in the electrical testing of modules and of the individual discrete components that go into the modules.

Another desirable quality of the MOSFET is that it is a voltage (not current) operated device. The input impedance at its gate is many megohms, thus no steady state power is required to operate them as a logic function (e.g., it is not necessary to supply "base current").

The MOSFET essentially has no "offset" voltage; it acts like an open circuit when off and a resistor (less than 3K) when on. When off the leakage is very low. This feature is very useful in commutating devices.

Another unique propriety of the MOSFET is that it is symmetric (one can't tell the source from drain). This, of course, means that a simple monolithic logic block can be made from MOSFET's and can be arranged in many different logic configurations. The blocks used are as follows:



It is left to the designer to utilize the many ways that the blocks can be connected and he will be pleasantly surprised at the things he can do with MOSFET logic blocks with very few parts and with considerable power savings.

On some occasions transistors are required and can be mated very nicely with MOSFET logic when required.

The writer is not qualified to comment on semiconductor manufacturing processes, but has been assured by competent personnel that the manufacturing process steps required to make an all MOSFET monolithic chip are considerably fewer than those for conventional integrated circuits. The two basic MOSFET blocks are made by the General Micro Electronics Company (GME) in California. The cooperation received from that plant has been outstanding in that "prototype" blocks of both types were delivered within a month after they received our drawings (FIBS-2 Figure 7). The blocks worked very well and the above example is given to illustrate that the manufacturing processes must indeed be simpler than those of integrated circuits.

4. Evaluation of MOSFET Approach

The various stages in evaluating the MOSFET approach are and will be as follows:

a. Circuit Design Using Individual MOSFET's:

Several different binaries were designed and breadboarded at Goddard. These binaries were operated in an extremely simple system to check their noise rejection, and speed versus power profile. The one chosen is that shown on Drawing FIBS-2, Figure 7. The disadvantage of this binary is that it takes 12 MOSFET's and 4 resistors and that its standby power is twice that of other binaries breadboarded. The advantage gained is that it is a threshold double input direct coupled device that can be manufactured with no capacitors or diodes. Good speed versus power was not obtained with the breadboard due to excessive capacities but this problem was largely solved by GME in their monolithic package.

b. Specification for the Two Basic Building Blocks

It was decided to have the 12 MOSFET's of the binary in an integrated package and to mount the chip in a TO-5 header. The four resistors were to be placed external to the package for two basic reasons as follows:

(1) The speed versus power can be tailored and

(2) The MOS technology has not advanced to the point where it is practical to put large value MOS resistors on the chip. In addition, the binary cannot "deadhead" the line if the large value resistors are external.

The TO-5 package was chosen because it is easier to weld to than the flat pack.

c. System Check Using Many MOSFET's (Breadboard)

A representative encoding system has been breadboarded. This system is about two-thirds the functional complexity of IMP A and contains the circuits that produce the new functions to be used in IMP's F&G (e.g., sixteen level oscillators, A/D converter, "S-T" accumulators, etc.) It contains 127 binary blocks and 208 logic blocks with only 17 transistors. The breadboard was made with 8 pin "tube sockets" such that the production MOSFET's were "plugged" in as soon as they arrived. Breadboarding with MOSFET blocks turns out to be much nicer than with conventional design. The electrical design and MOSFET performance was evaluated with this system. The system worked very well indeed.

d. Welded MOSFET Encoding System Package

The breadboard MOSFET's were removed and were welded into a package (Delta Pack) and complete system checks have been performed using simulated experiment inputs. The package has been potted. The welded modules were layed out and fabricated by Goddard's Modular Techniques Section. The MOSFET card has been evaluated at T&E. The following tests were run, and the unit passed all successfully:

a) Initial magnetic tests
b) Acceleration tests
c) Vibration
d) Humidity
e) Thermal vacuum
f) Final magnetic tests

Modules for IMP D&E are now being fabricated.

PART III. IMP D&E ENCODER INTERFACES

AMES MAGNETOMETER INTERFACE

The Ames Magnetometer experiment will read out 30 analog samples during channels 1 through 15 of frames 0, 4, 8 and 12 and digital data flags will be read in channel 12 of frame 7.

1. The analog voltage data line, called "Ames In" will vary between ground and +5 volts with an output impedance less than 1 K ohm. The experimenter shall insure that the voltage never exceeds +5.5 volts and does not go more negative than -0.5. Variation during readout burst less than .5% is required for accurate data processing.

2, 3, 4, and 5. The digital data flag lines will be defined in the following manner:

> The "true state" will be defined when level is 0 V +.25, -3 volts, this will be encoded as a "0"
>
> The "false state" will be defined when 5 V +1, -2 volts, this will be encoded as a "1"

Bit I is least significant and Bit IV is most significant.

The data flags will mean:

a. Calibrate flag and perm. bit 2

b. Flipper flag and perm. bit 3

c. Channel switch flag and perm. bit 4

d. Perm. bit 1 and perm. bit 5.

One set of flags will be gated by the experiment onto the four lines during the first half of every channel, and the other set of flags will be gated, by the experiment, onto the four lines during the second half of every channel.

The synchronization pulses will be more negative than -2 volts through 100 K ohms during the specified time, and more positive than +5.5 volts through 200 K ohms at all other times. (See II-E)

The synchronization lines required are:

6. "4S" $\frac{200}{(16 \text{ cps})}$ square wave, positive at beginning of channel

7. "2S" $\frac{100}{(16 \text{ cps})}$ square wave, positive at beginning of channel

8. "S" $\frac{50}{(16 \text{ cps})}$ square wave, positive at beginning of channel

9. "H" square wave, positive at beginning of channel

10. "G" square wave, positive at beginning of frame

11. "F" square wave, positive at beginning of frame

12. "E" square wave, positive at beginning of frame

13. "D" square wave, positive at beginning of sequence

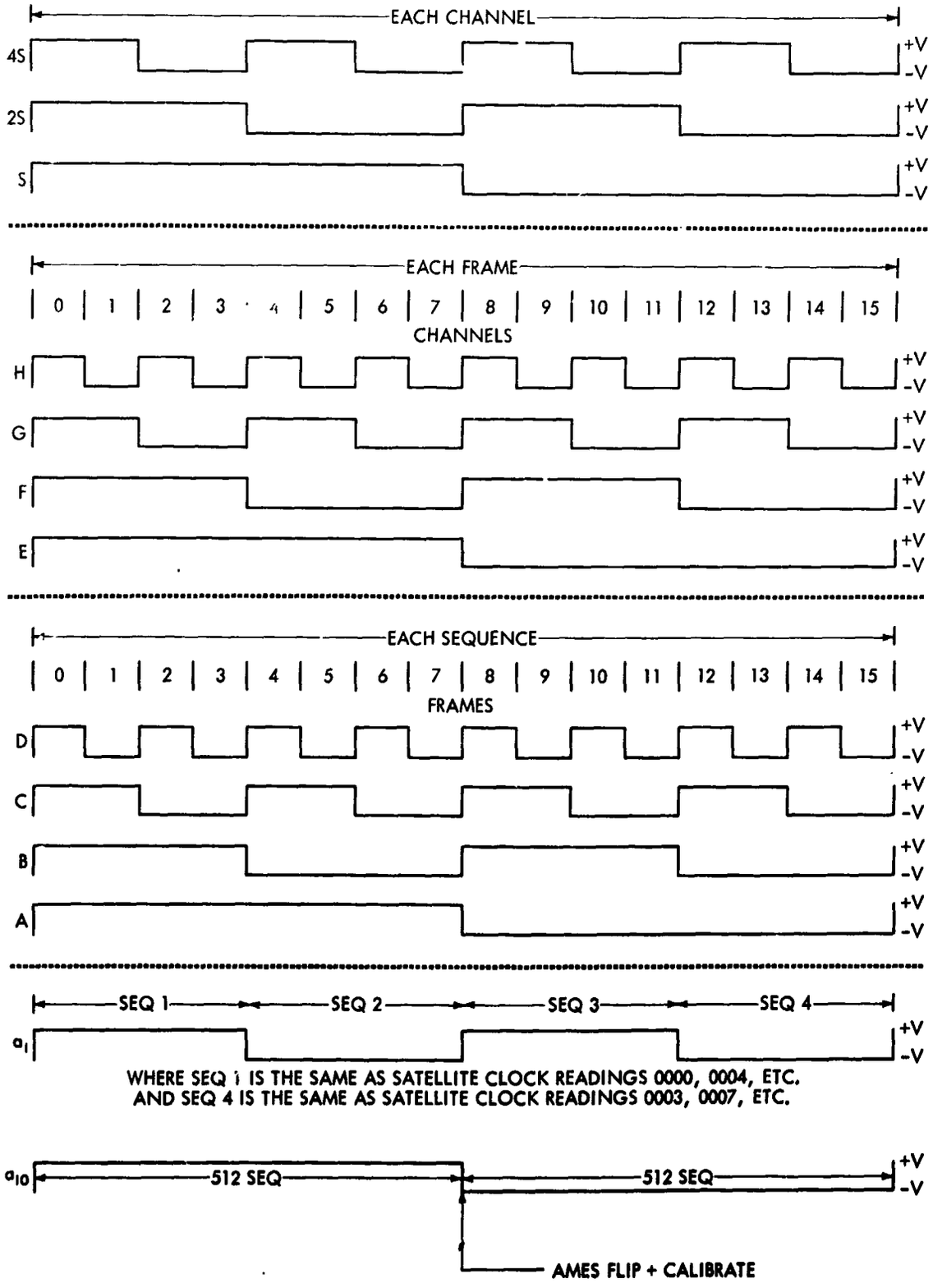
14. "C" square wave, positive at beginning of sequence

15. "a_{10}" square wave period approximately 23 hours

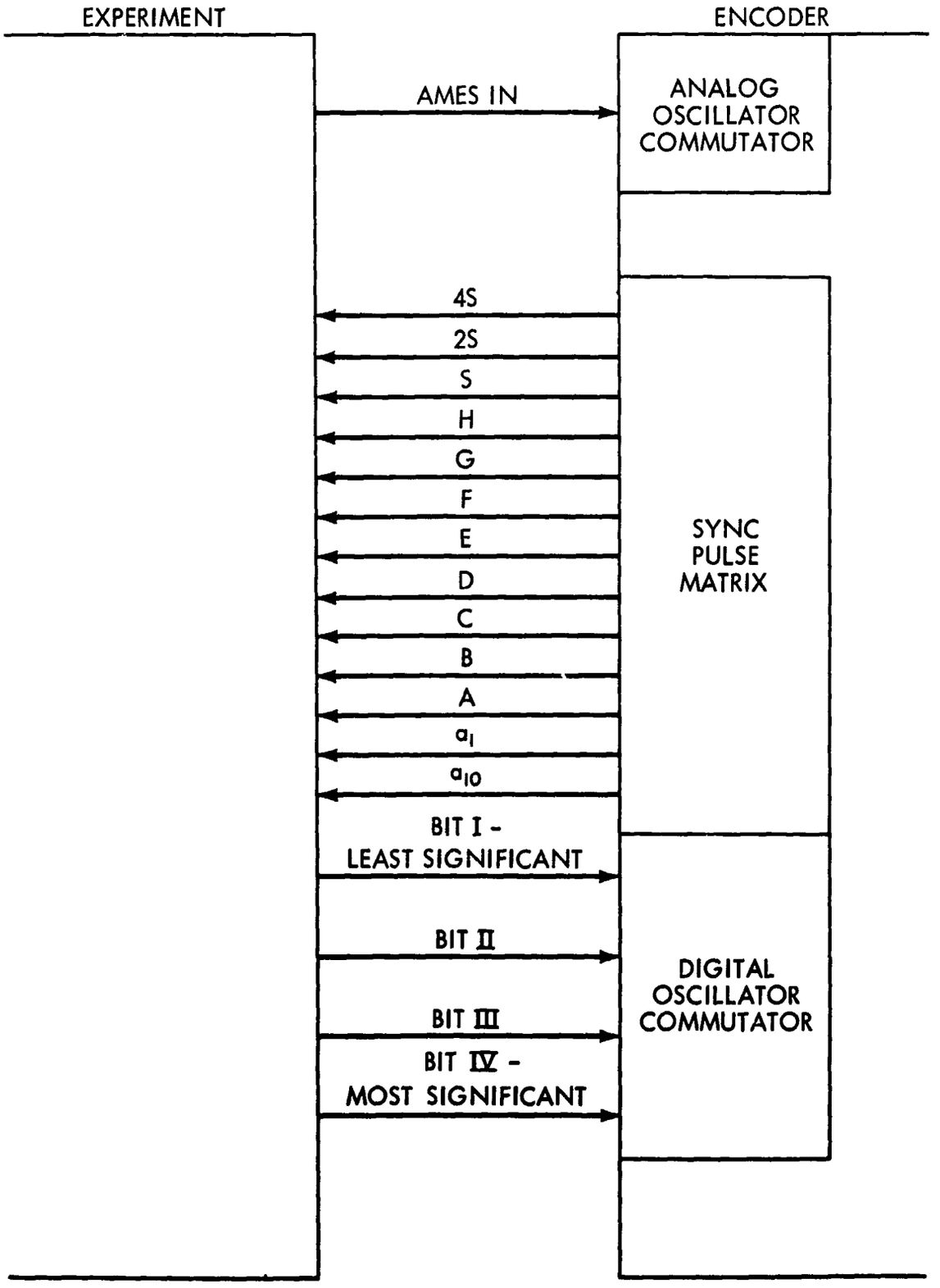
16. "B" square wave, positive at beginning of sequence

17. "A" square wave, positive at beginning of sequence

18. "a_1" square wave period of two sequences.



Ames Sync Pulses



Ames Interface Diagram

UNIVERSITY OF IOWA INTERFACE

The University of Iowa Experiment is allocated eight accumulators in the DDP as defined below.

	Accumulator	Number of Bits	Readout In		Maximum Count Rate (KC)
			Channels	Frames	
1.	1a	20	4, 5, 1/2(6)	1, 9	250
2.	1b	12*	1/2(6), 7	1, 9	250
3.	2a	20	12, 13, 1/2(14)	1, 9	250
4.	2b	12*	1/2(14), 15	1, 9	250
5.	3a	20	4, 5, 1/2(6)	3, 11	250
6.	3b	12**	1/2(6), 7	3, 11	250
7.	4a	20	12, 13, 1/2(14)	3, 11	250
8.	4b	12**	1/2(14), 15	3, 11	250

Each accumulator will be reset after every readout, in groups of 32 bits.

Pulse duration will be between 2 and 3 μseconds.

The synchronization pulses will be more negative than -2 volts through 100 K ohms during the specified time, and more positive than +5.5 volts through 200 K ohms at all other times. (See II-E.)

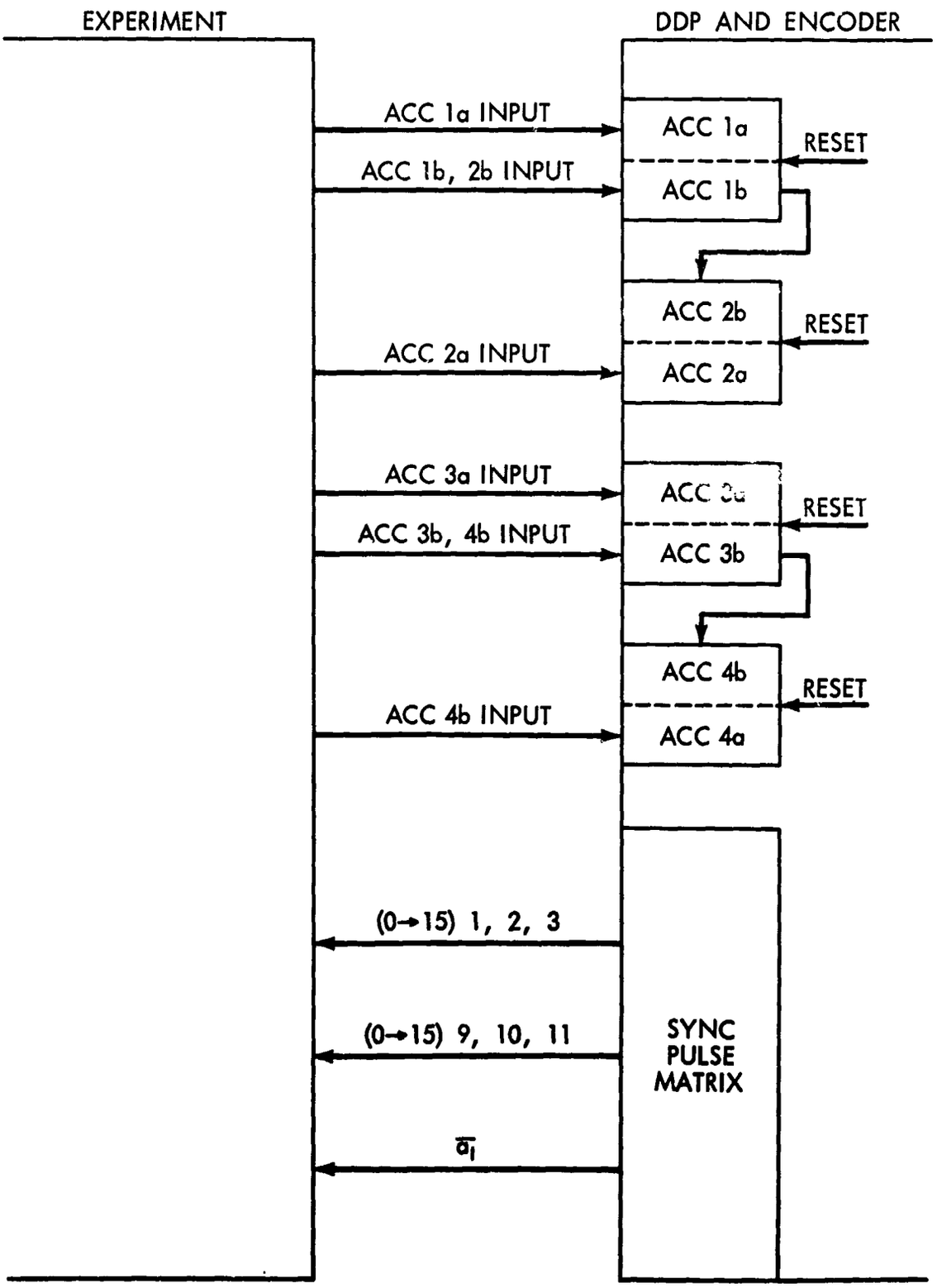
The synchronization pulses required are:

9. $\overline{a}_1$
10. Channel (0 ⟶ 15) - Frame 1, 2, 3
11. Channel (0 ⟶ 15) - Frame 9, 10, 11

The accumulator input pulses are counted when they change from ground to a voltage greater than +3 volts. The voltages should not exceed +7

*The readout of 1b represents the least significant 12 bits and readout of 2b represents the most significant 12 bits of a 24 bit accumulator.

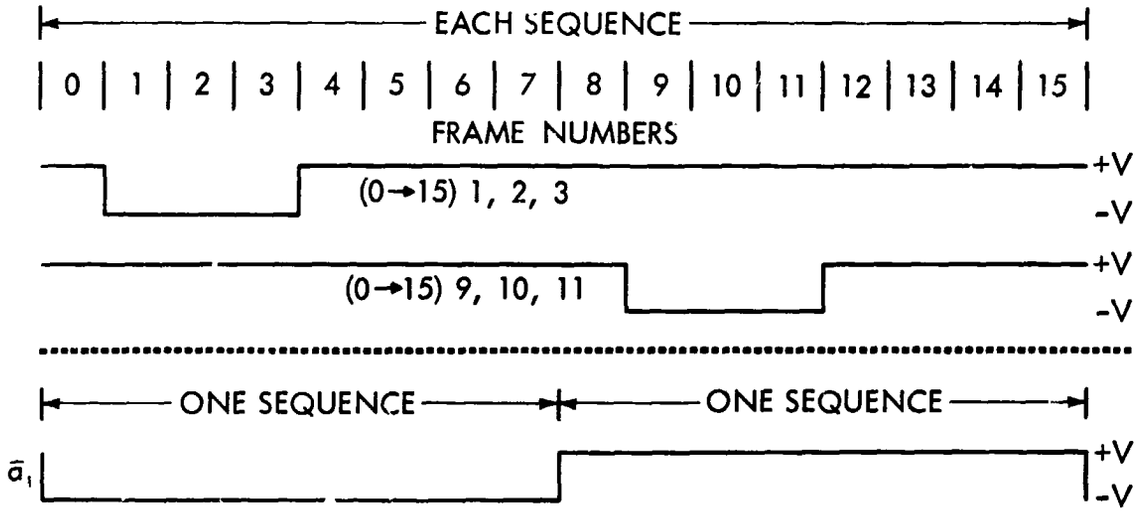
**The readout of 3b represents the least significant 12 bits and readout of 4b represents the most significant 12 of a 24 bit accumulator.



University of Iowa Interface

volts or -3 volts at the accumulator input. The accumulator input impedance will be at least 10K ohms.

The experiment must not allow pulses to activate line "1b, 2b in" during channels 4 ⟶15 of frames 1 and 9 or line "3b, 4b in" during channels 4 ⟶15 of frames 3 and 11 as erroneous readout of the accumulators will occur. See Section IV-D for encoder freeze information of all accumulators.



University of Iowa Sync Pulses

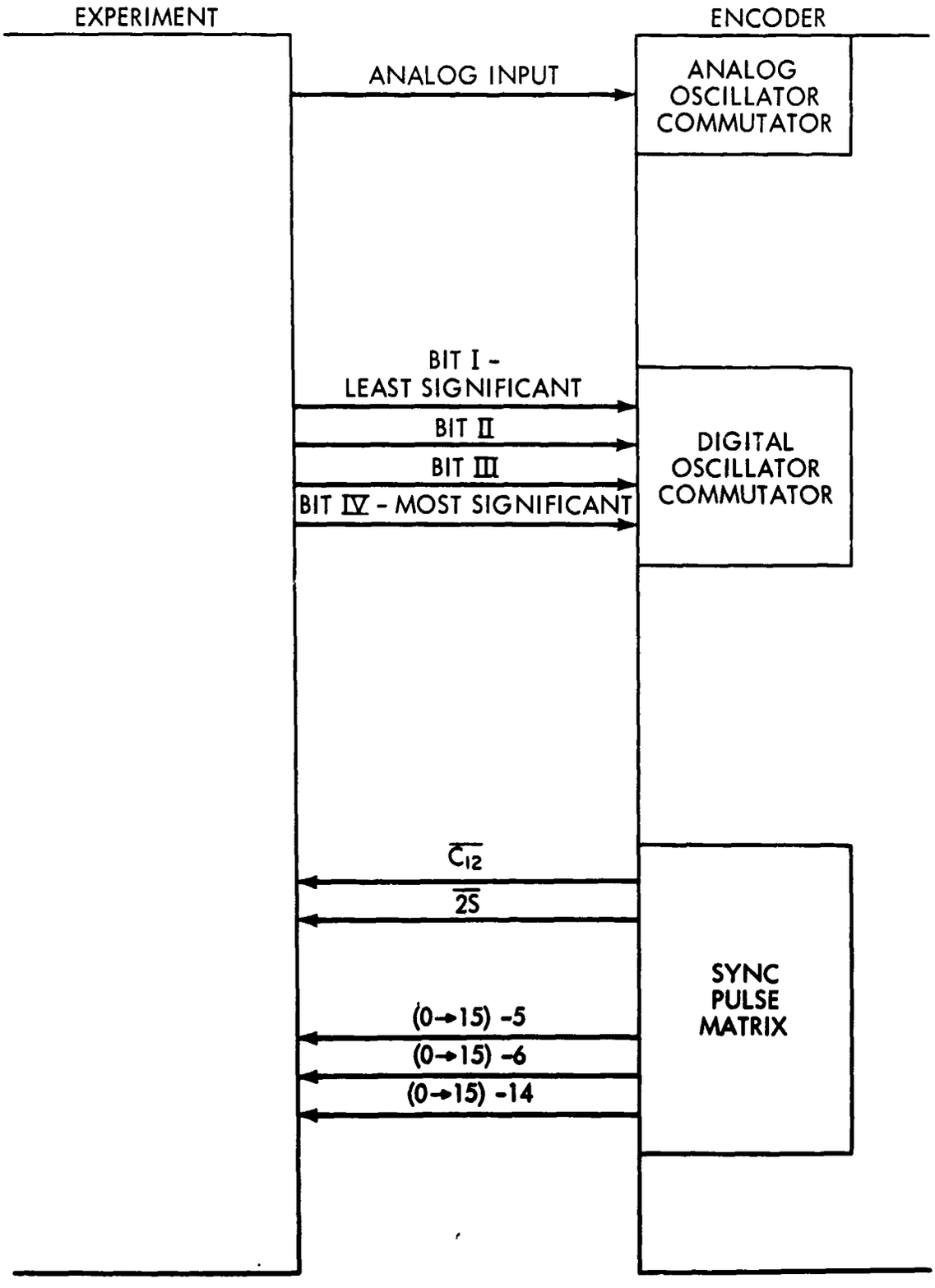
MASSACHUSETTS INSTITUTE OF TECHNOLOGY INTERFACE

The MIT experiment will read out 30 analog samples during channels 1 through 15 of frame 6 and 30 4-bit digital words during channels 1 through 15 of frame 14.

1. **The analog voltage data line, called "MIT IN" will vary between ground and +5 volts with an output impedance less than 1 K ohm. This voltage shall not be able to exceed +5.5 volts or -3 volts (limiting to be done in experiment). Variation during readout should be less than .5%.**

2, 3, 4 and 5. **The digital data lines will be defined as follows: One state will be defined when near ground. The other state will be defined when greater than +3 volts. (See p. 14) Bits to be held constant during each burst, within 100 μ seconds after burst begins.**

Bit I is least significant and Bit IV is most significant.



Massachusetts Institute of Technology Interface

The synchronization pulses will be more negative than -2 volts through 100 K ohms during the specified time, and more positive than +5.5 volts through 200 K ohms at all other times. (See II-E)

The synchronization lines required are:

6. $\overline{C_{12}}$ - 50 cps square wave, negative at the beginning of each data burst.

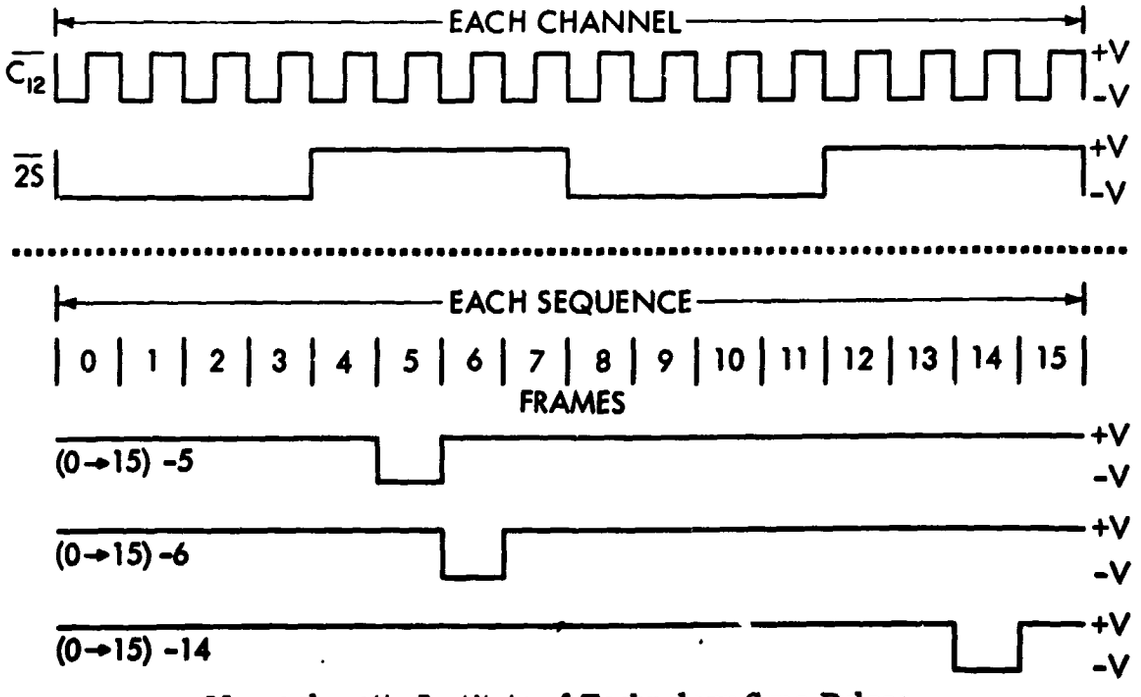
7. $\overline{2S}$ - 50/8 cps square wave, negative at the beginning of each data burst.

8. $\overline{S}$ - 50/16 cps square wave, negative at the beginning of each channel. (Unused in AIMP D; used by thermal ion and electron experiment in AIMP E)

9. (0 ⟶ 15) - 6 - negative during all of frame 6.

10. (0 ⟶ 15) - 14 - negative during all of frame 14.

11. (0 ⟶ 15) - 5 - negative during all of frame 5.



Massachusetts Institute of Technology Sync Pulses

THERMAL ION AND ELECTRON INTERFACE FOR AIMP D
TEMPLE UNIVERSITY INTERFACE FOR AIMP E

The Temple University Experiment digital data will be scanned during channels 5, 6, and 7 of frames 7 and 15. Four bits will be scanned during each half of the channel. These bits shall be shifted and held steady within 100 microseconds by the experiment after the shift command is sent. (See p. 10)

1, 2, 3 and 4. The digital data lines are defined in the following way:

One state will be defined when near ground. The other state will be defined when greater than +3 volts. (See p. 14)

Bit I is least significant and Bit IV is most significant.

Synchronization pulses will be supplied more negative than -2 volts through 100 K ohms during the specified time, and more positive than +5.5 volts through 200 K ohms at all other times. The pulses are:

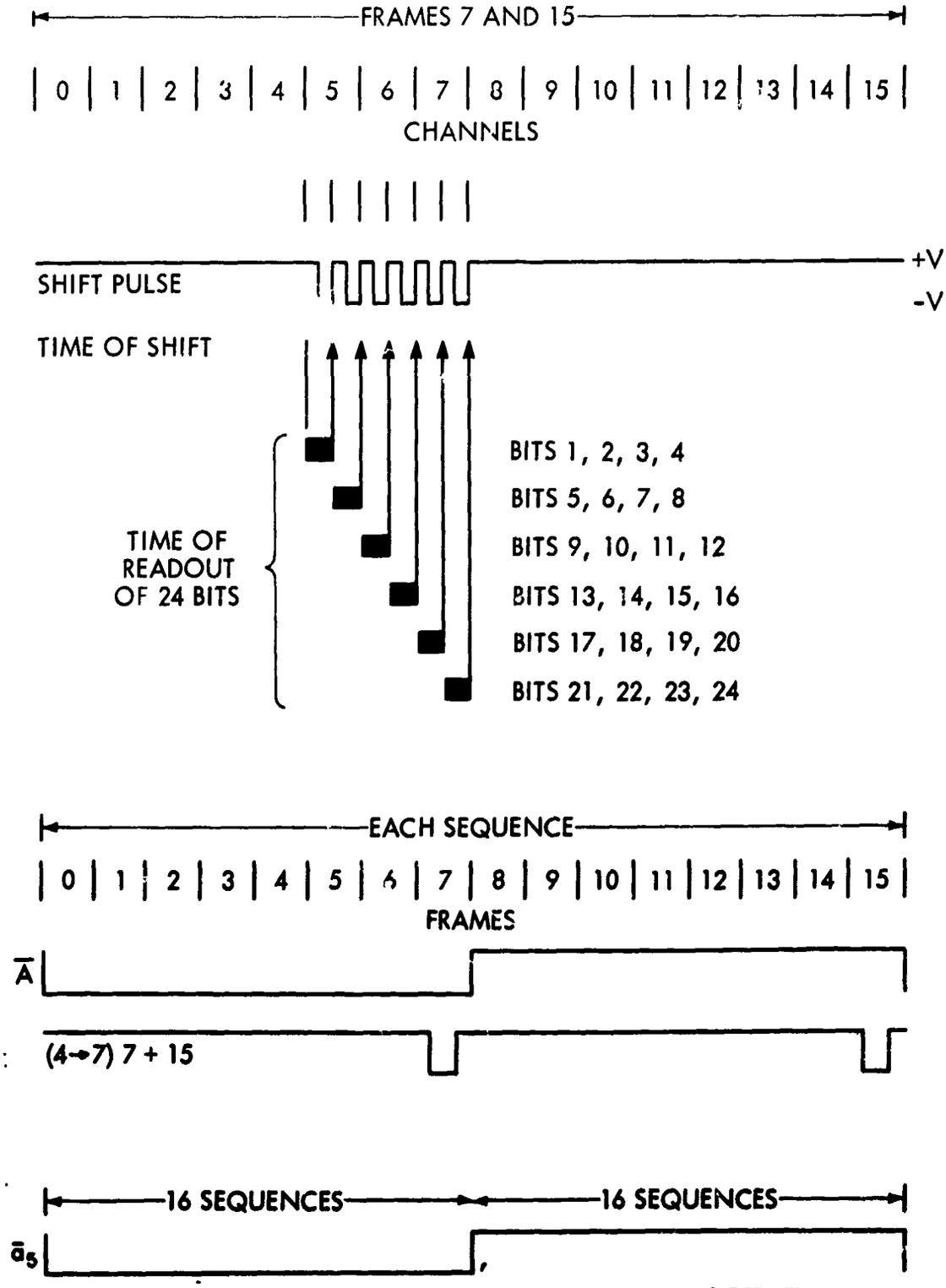
5. Channel 4 ⟶ 7 of frames 7 and 15 (B. C. D. $\overline{F}$. F.) will be negative only during the second quarter of frames 7 and 15 (to be used to inhibit experiment during readout).

6. $\overline{A}$ negative during first half of sequence.

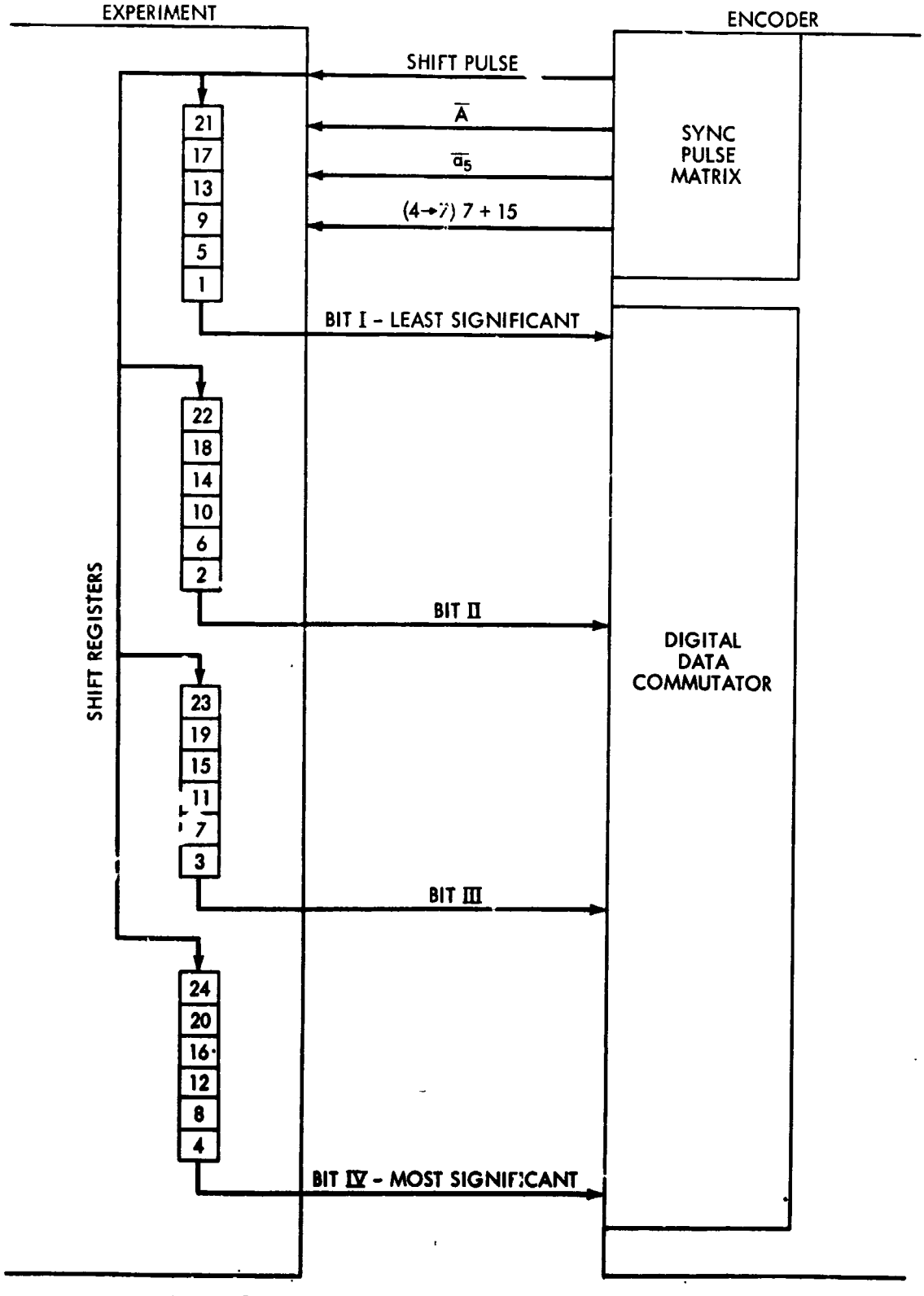
7. $\overline{a_5}$ 32 seq. period

8. Shift pulse.

A shift pulse will be supplied to the experiment, changing from a voltage more negative than -2 volts through 1.0 K ohms and rising to a voltage more positive than +5 volts through 20 K ohms. The output is an emitter follower with 20 K ohms output series resistor. The shift operation is to be performed when the level shifts from negative to positive. The shift pulse should not be directly differentiated because of possible noise on the shift line causing interference.



Thermal Ion (AIMP D) & Temple Sync Pulses (AIMP E)



Thermal Ion (AIMP D) & Temple Interface (AIMP E)

UNIVERSITY OF CALIFORNIA INTERFACE

The University of California experiment will feed four accumulators as defined below:

	Accumulator	Type	Accumulator Speed (KC)	Readout In	
				Channels	Frames
1.	5a - 16 bit	S-T	100	4 & 5	5, 13
2.	5b - 16 bit	Count	10	6 & 7	5, 13
3.	6a - 16 bit	S-T	100	12 & 13	5, 13
4.	6b - 12 bit*	Count	10	14 1/2 & 15	5, 13

Accumulator 5 will be reset after channel 7 on frames 5 and 13.

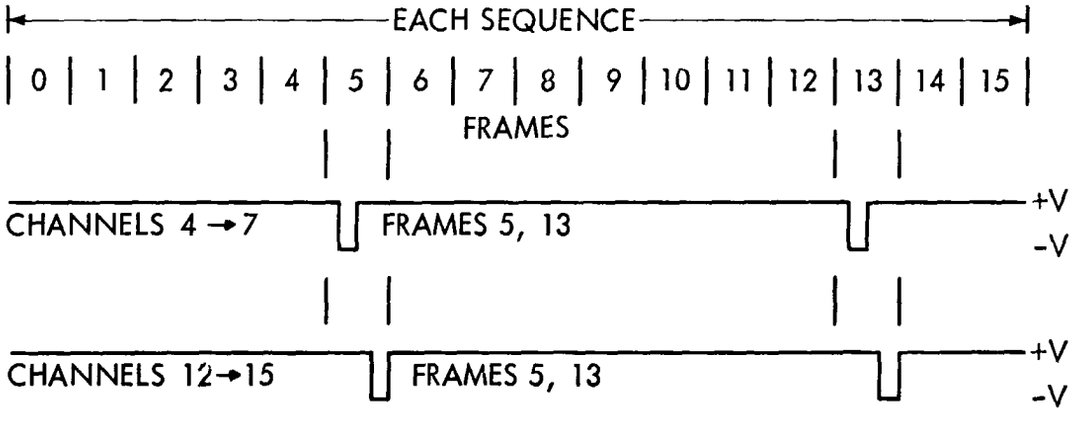
Accumulator 6 will be reset after channel 15 on frames 5 and 13.

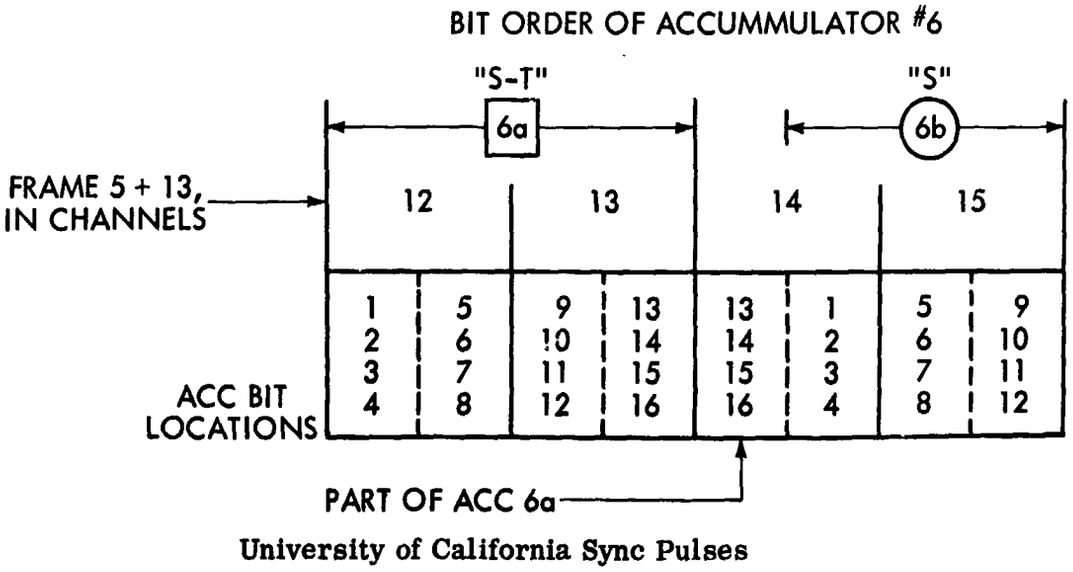
The synchronization pulses will be more negative than -2 volts through 100 K ohms during the specified time, and more positive than +5.5 volts through 200 K ohms at all other times. The sync pulses required are: (See II-E)

1. C_7 - 1.6 kilocycle square wave
2. (Channel 4 ⟶ 7) Frames 5 and 13
3. (Channel 12 ⟶ 15) Frames 5 and 13

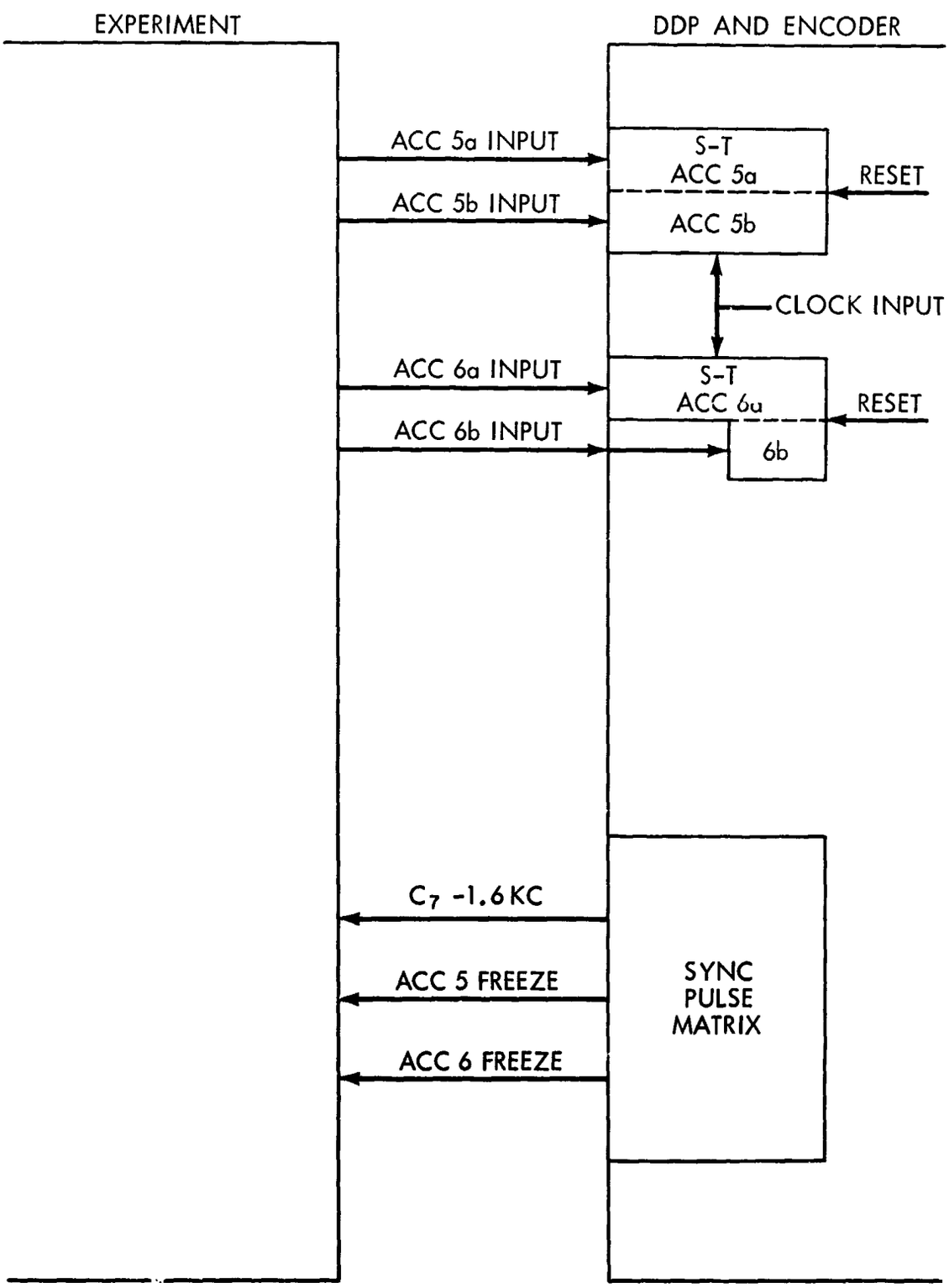
The accumulator input pulses are counted when they change from ground to a voltage greater than +3 volts. The voltages should not exceed +7 volts or -3 volts at the accumulator input. The accumulator input impedance will be at least 10 K ohms. The accumulator input pulses will be 2 μsecond or greater. (See IV-C)

*The position in the telemetry format for the first four bits of acc. #6b will be used to repeat the four most significant bits of accumulator 6a.





University of California Sync Pulses



University of California Interface

GODDARD MAGNETOMETER INTERFACE

The Goddard Magnetometer experiment will be scanned on four digital data lines. The four digital data lines will be defined in the following way:

"0" state will be defined when near ground.

The "1" state will be defined when greater than +3 volts. (See p. 14)

Bit I is least significant and Bit IV is most significant.

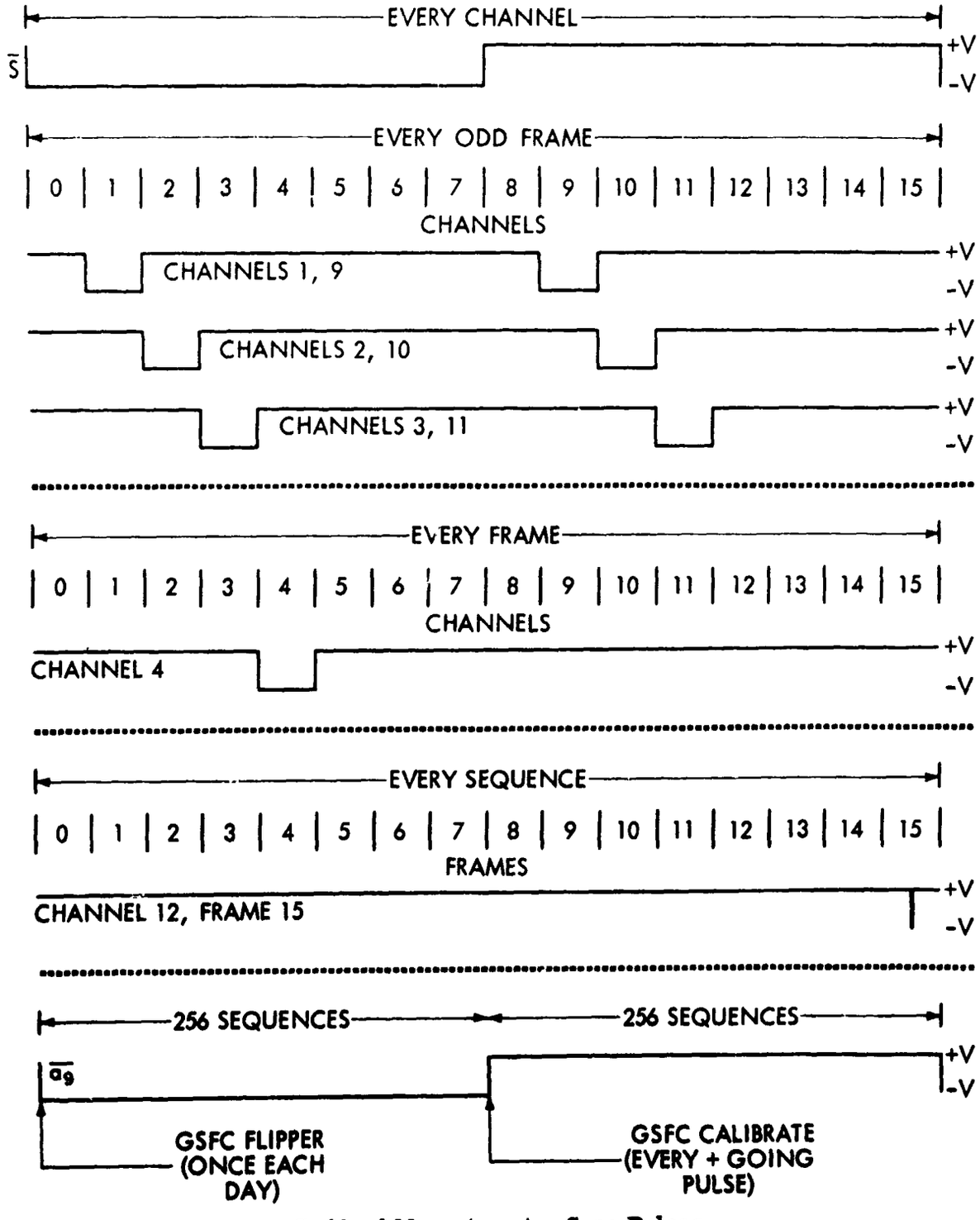
Bits should not change during readout.

The encoder input impedance will be greater than 20 K ohms.

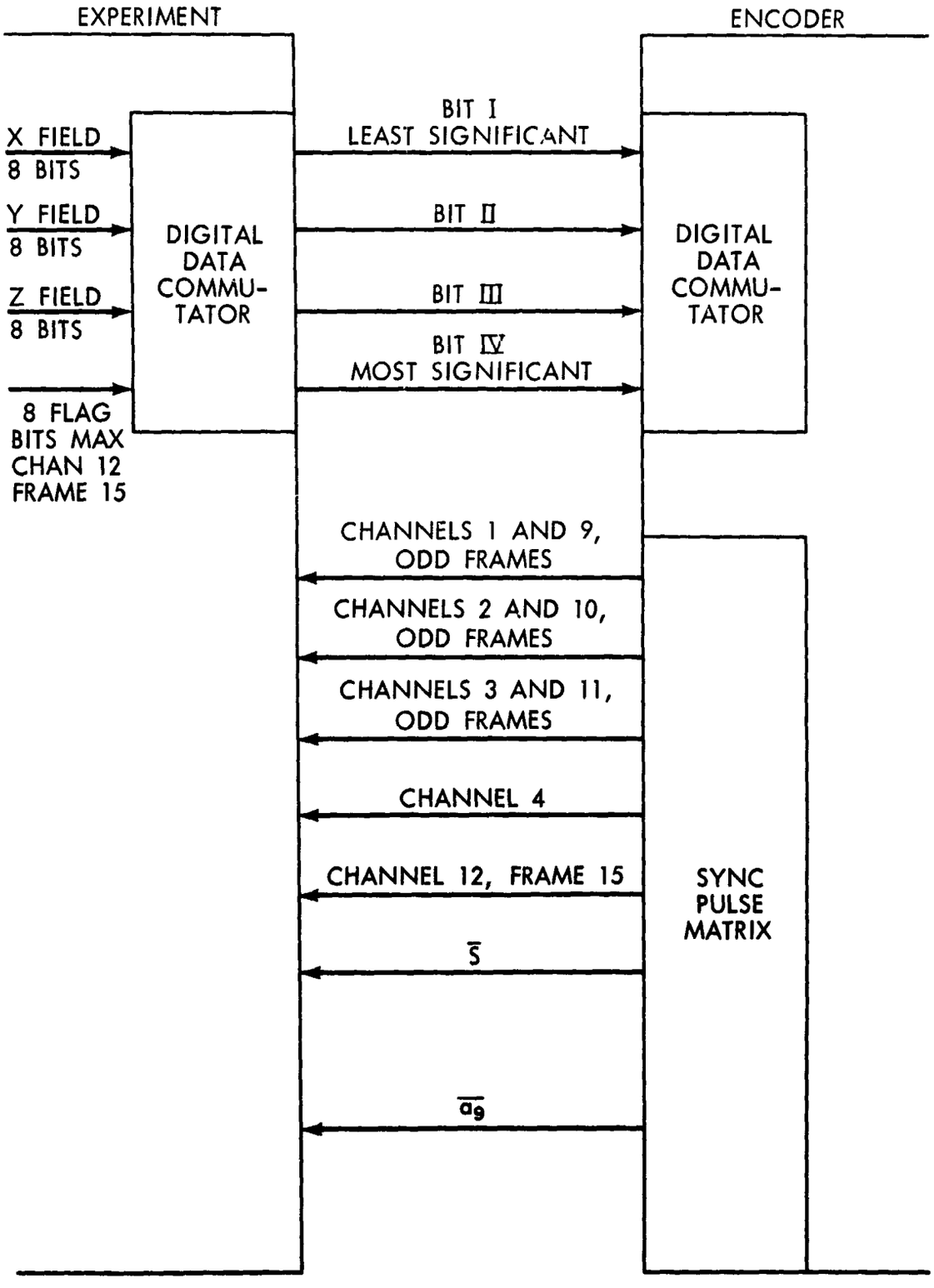
The synchronization pulses will be more negative than -2 volts through 100 K ohms during the specified time and more positive than +5.5 volts through 200 K ohms at all other times. (See II-E)

The sync pulses supplied by the encoder will be:

1. Channel 1 and 9, every odd frame.
2. Channel 2 and 10, every odd frame.
3. Channel 3 and 11, every odd frame.
4. Channel 4 every frame.
5. Channel 12 frame 15.
6. $\overline{S}$ - negative during first half of every channel and positive during the second half.
7. $\overline{A}$ - negative for first half of every sequence, positive for second half of every sequence. (unused AIMP D; used by thermal ion exp. on AIMP E)
8. $\overline{a_9}$ - negative for 256 sequences, positive for next 256 sequences.



Goddard Magnetometer Sync Pulses



Goddard Magnetometer Interface

OPTICAL ASPECT INTERFACE

The optical aspect detector will shift 120 digital bits, four bits per half channel, onto four digital data lines. These bits shall be shifted within 100 microseconds after the shift command is sent and held steady until the next shift command is sensed. The digital data lines will be defined as on page 14, except the maximum voltage will be 3.5 volts. Minimum for "1" state will be +1.0 volts into the 10K base resistor, "0" state at ground to +.5 volts.

Bit I is least significant and Bit IV is most significant.

The synchronization pulses will be supplied more negative than -2 volts through 50K ohms during the specified time, and more positive than +5.5 volts through 100K ohms at all other times. (See II-E)

The pulses to be supplied are:

1. Clock pulse 800 cps - C_8.

2. Clock pulse 6.4 KC - C_5.

3. $(Ps)_1$ (Channel 0 ⟶ 15) (0 ⟶ 2, 8 ⟶ 10) sequence 1, 2, 3 FR (0 ⟶ 2, 10) sequence 4.

4. $(Ps)_2$ (All of FR 0, 1, 2, 10) Seq 1 & 3, (All of FR 2, 10) Seq 2 & 4.

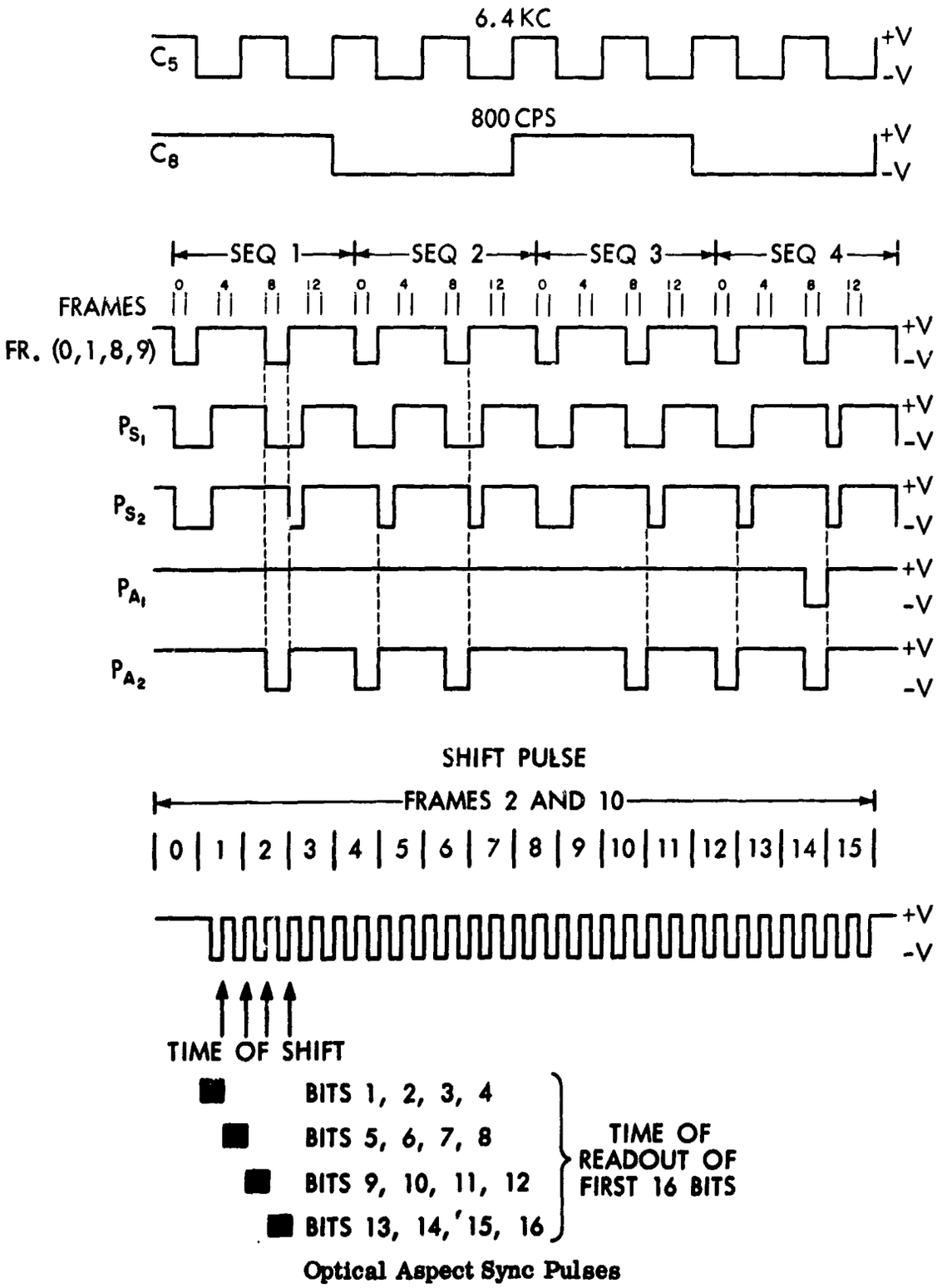
5. $(Pa)_1$ (Channel 0 ⟶ 15) (8 & 9) sequence 4.

6. $(Pa)_2$ (All of FR 8, 9) Seq 1 & 3, (All of FR 0, 1, 8, 9) Seq 2 & 4.

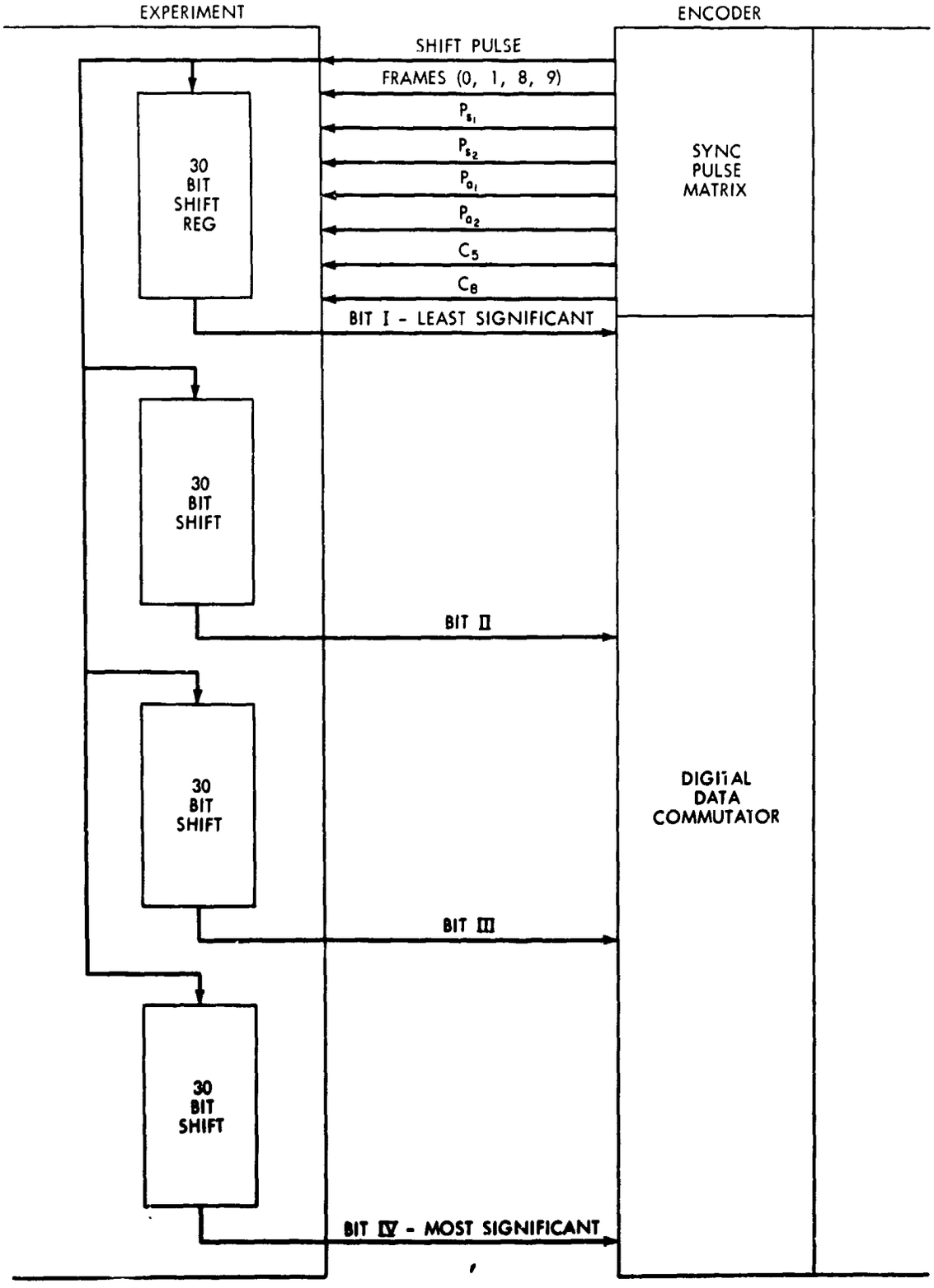
7. Channel (0 ⟶ 15) FR (0, 1, 8, 9).

A shift pulse will be supplied to the experiment, changing from a voltage more negative than -2 volts through 20K ohms and rising to a voltage more positive than +5 volts through 20K ohms. The output is an emitter follower with 20K ohms output resistor.

The shift operation is to be performed when the level shifts from negative to positive. The shift pulse should not be directly differentiated because of possible noise on the shift line causing interference. (See II-C-4)



Optical Aspect Sync Pulses



Optical Aspect Interface

ADDITIONAL OPTICAL ASPECT INFORMATION

A parity check of the optical aspect data will be attempted within the encoder. This check will not only check the quality of the data when all is present, but will also allow single missing data points within a group of data to be corrected with a high degree of certainty, as shown in the following table:

Parity Symbol	Data to be Checked	Approx. % of Data to be Thrown Out	Approx. P (double error)	Approx. P (correction)
PC_1	FR2, CH(1 ⟶ 7)	1500 Pe	.50 Pe^2	Pe
PC_2	FR2, CH(8 ⟶ 15)	1700 Pe	.54 Pe^2	Pe
PC_3	FR10, CH(1 ⟶ 7)	1500 Pe	.50 Pe^2	Pe
PC_4	FR10, CH(8 ⟶ 15)	1700 Pe	.54 Pe^2	Pe

Where Pe = probability of wrongly digitized data

P (double error) = probability of not detecting a double error when all data points are digitized

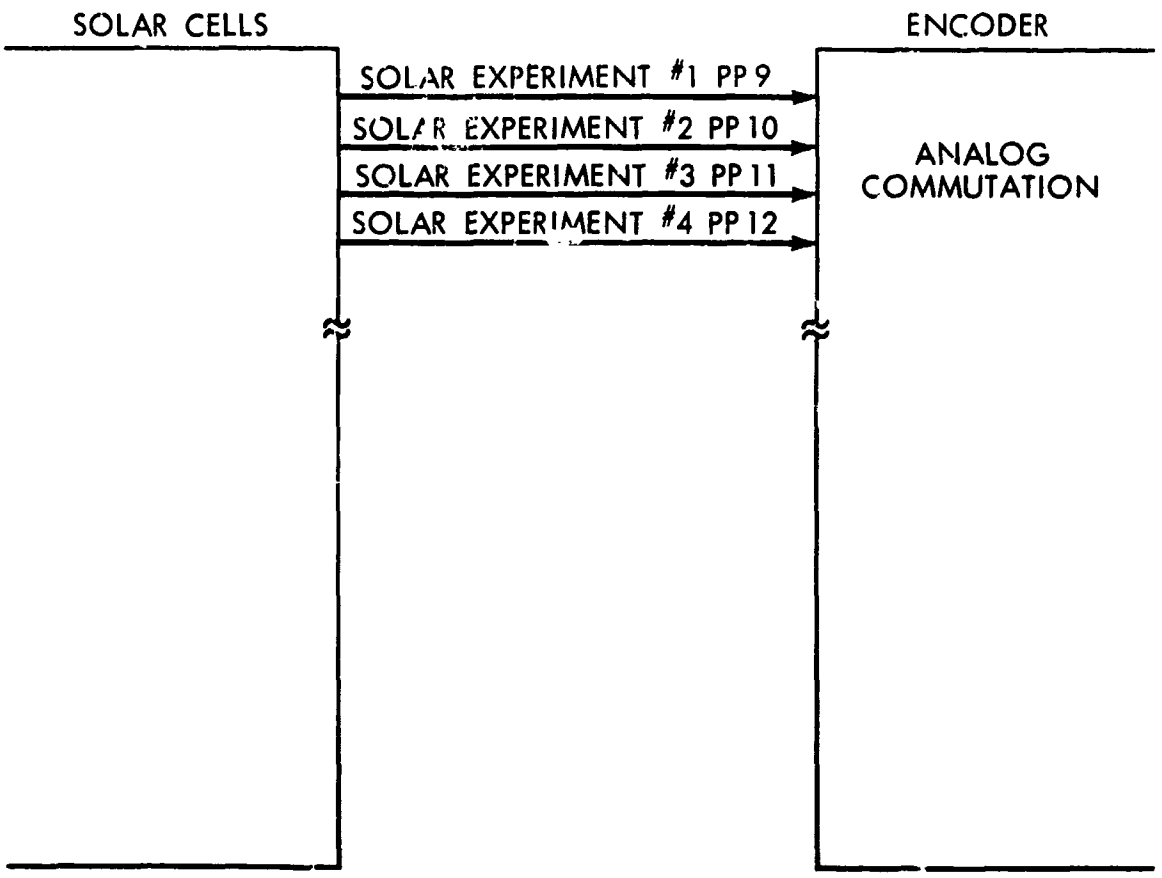
P (correction) = probability of inserting the proper information for one missing data point.

For IMP D, the value of Pe if comb filters are used in signal detection is very much less than .01 (if correlators are used, the value should still be less than .01). If the value of Pe were .01, then 15% of the data would be thrown out to give the remaining data about .00006 probability of being in error. The probability of incorrectly inserting the information in a missing data point should be about .01.

INTERFACE WITH SOLAR CELL EXPERIMENT

The solar cells will produce voltages from 0 volts to +5 volts with impedances less than 100 ohms. The four output lines will be fed into the analog commutator, and be digitized before being transmitted as performance parameters during the second sequence. Thus, they will be transmitted once every four sequences, as four, 8-bit words.

	Read Out
PP_9	Seq. 2 FR1
PP_{10}	Seq. 2 FR3
PP_{11}	Seq. 2 FR5
PP_{12}	Seq. 2 FR7



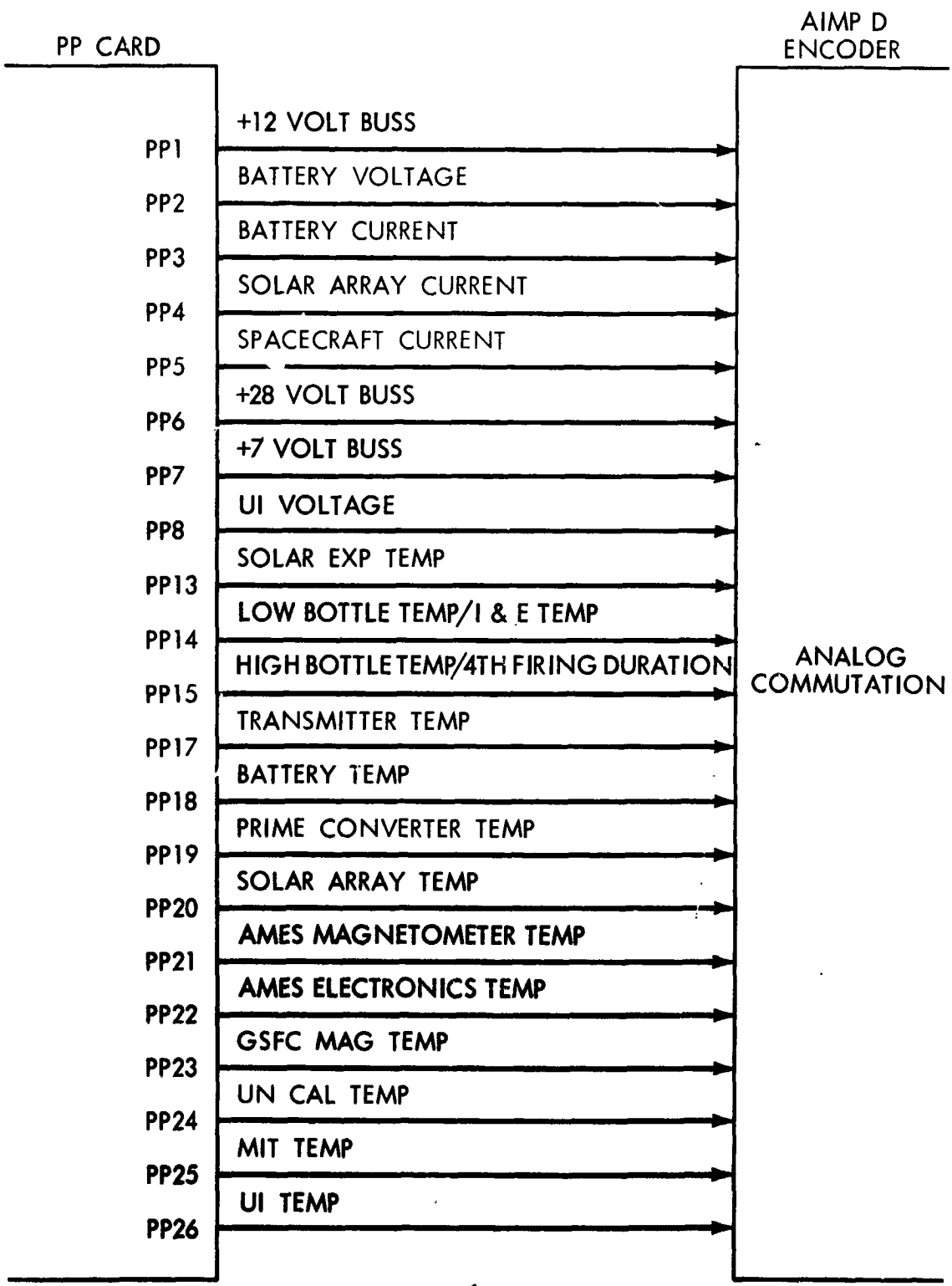
Interface with Solar Cell Experiment

INTERFACE WITH PERFORMANCE PARAMETER CARD

The lines shown on the next page will vary between 0 and +5 volts with impedances less than 15 K ohms. The analog commutator will select the proper parameter, which is fed to the analog oscillator. An 8-bit accumulator is gated on for 20 milliseconds in channel 0 and readout in channel 8 of each even frame. (See II-D)

Channel 8 (8 bits each) - Digitized Analog			
Frame No.	Sequence 1	Frame No.	Sequence 3
1	PP1, +12 volt Buss	1	PP1, +12 volt Buss
3	PP2, Battery Voltage	3	PP2, Battery Voltage
5	PP3, Battery Current	5	PP3, Battery Current
7	PP4, Solar Array Current	7	PP4, Solar Array Current
9	PP5, Spacecraft Current	9	PP5, Spacecraft Current
11	PP6, +28 volt Buss	11	PP17, Transmitter Temperature
13	PP7, +7 volts Temperature PP's	13	PP18, Battery Temperature
15	PP8, UI voltage	15	PP19, Prime Converter Temperature
	Sequence 2		Sequence 4
1	PP9, Solar Experiment 1	1	PP20, Solar Array Temperature
3	PP10, Solar Experiment 2	3	PP21, Ames Temperature 1
5	PP11, Solar Experiment 3	5	PP22, Ames Temperature 2
7	PP12, Solar Experiment 4	7	PP23, GSFC Magnetometer Temperature
9	PP13, Solar Experiment Temperature	9	PP24, UCAL Temperature
11	PP14, Low Bottle Temperature/Temple Temperature	11	PP25, MIT Temperature
13	PP15, High Bottle Temperature/Fourth Stage Firing Time	13	PP26, UI Temperature
15	PP16, Encoder Oscillator Calibration	15	PP16, Encoder Oscillator Calibration

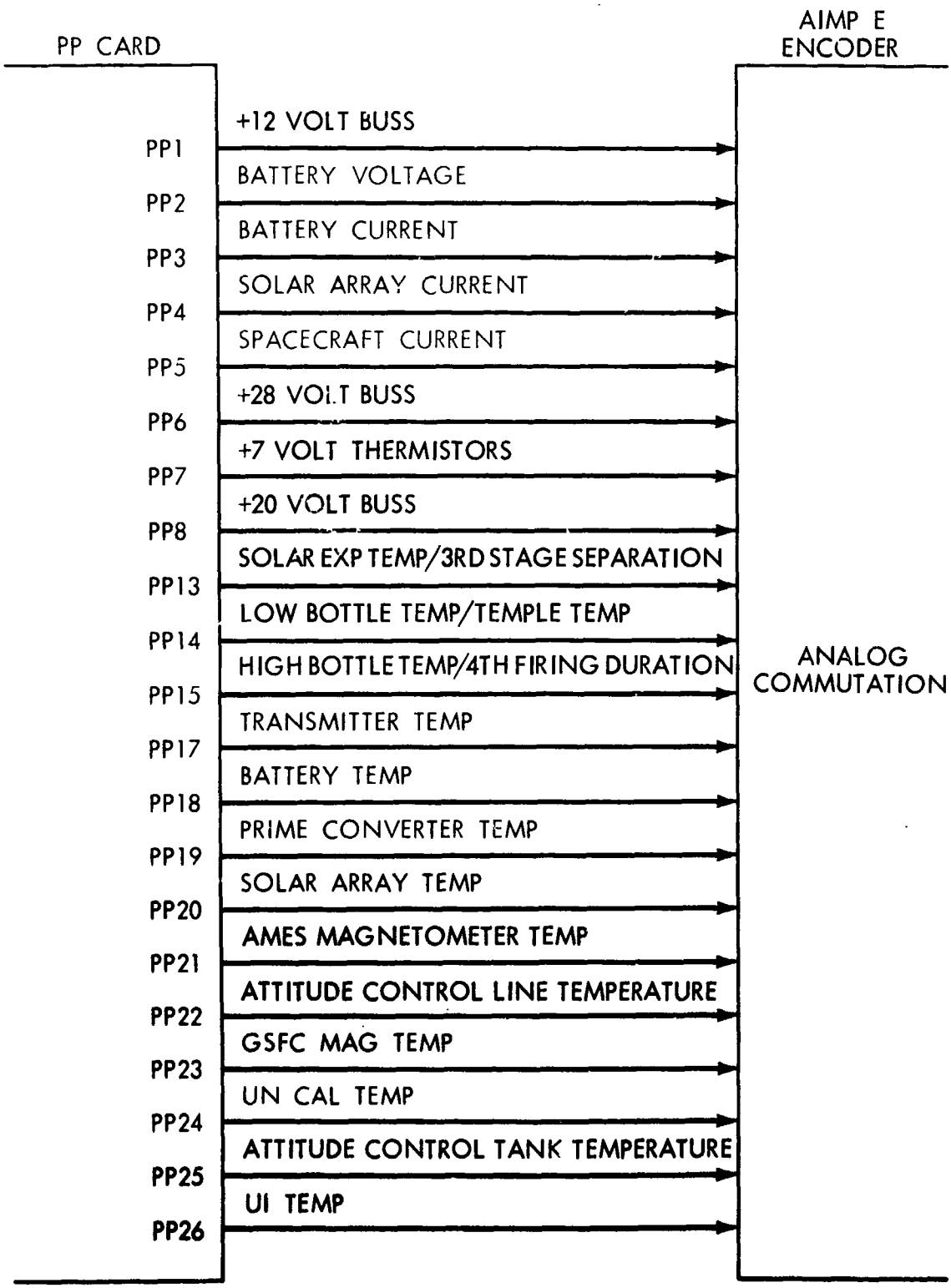
IMP-D
Performance Parameter Assignments



AIMP D
Interface with Performance Parameter Card

Channel 8 (8 bits each) - Digitized Analog			
Frame No.	Sequence 1	Frame No.	Sequence 3
1	PP1, +12 volt Buss	1	PP1, +12 volt Buss
3	PP2, Battery Voltage	3	PP2, Battery Voltage
5	PP3, Battery Current	5	PP3, Battery Current
7	PP4, Solar Array Current	7	PP4, Solar Array Current
9	PP5, Spacecraft Current	9	PP5, Spacecraft Current
11	PP6, +28 volt Buss	11	PP17, Transmitter Temperature
13	PP7, +7 volt Thermistors	13	PP18, Battery Temperature
15	PP8, +20 volt Buss	15	PP19, Prime Converter Temperature
	Sequence 2		Sequence 4
1	PP9, Solar Experiment 1	1	PP20, Solar Array Temperature
3	PP10, Solar Experiment 2	3	PP21, Ames Magnetometer Temperature
5	PP11, Solar Experiment 3		
7	PP12, Solar Experiment 4	5	PP22, AC Line Temperature
9	PP13, 3rd Stage Separation/ Solar Experiment Temperature	7	PP23, GSFC Magnetometer Temperature
		9	PP24, UCAL Temperature
11	PP14, Low Bottle Temperature/Temple Temperature	11	PP25, Attitude Control Tank Temperature
13	PP15, High Bottle Temperature/Fourth Stage Firing Time	13	PP26, UI Temperature
15	PP16, Encoder Oscillator Calibration	15	PP16, Encoder Oscillator Calibration

IMP-E
Performance Parameter Assignments



AIMP E
Interface with Performance Parameter Card

INTERFACE WITH PROGRAMMER CARDS

The binary performance parameters will have the following characteristics:

A voltage more positive than 3 volts into a 20 K ohm encoder impedance will represent "One" state.

A voltage more negative than +.5 volts of ground will represent the "0" logic state.

1. 4th stage ignition timer #1 1st decade (first burst, bit I)

2. 4th stage ignition timer #1 2nd decade (first burst, bit II)

3. Separation Armed (first burst, bit IV)

4. 4th stage ignition timer #2 1st decade (second burst, bit I)

5. 4th stage ignition timer #2, 2nd decade (second burst, bit II)

6. Separation Armed (second burst, bit IV)

The following sync pulses supplied to the programmer will vary from a voltage more positive than 5 volts at 10 K ohms output impedance to a voltage more negative than ground at 110 K ohms output impedance:

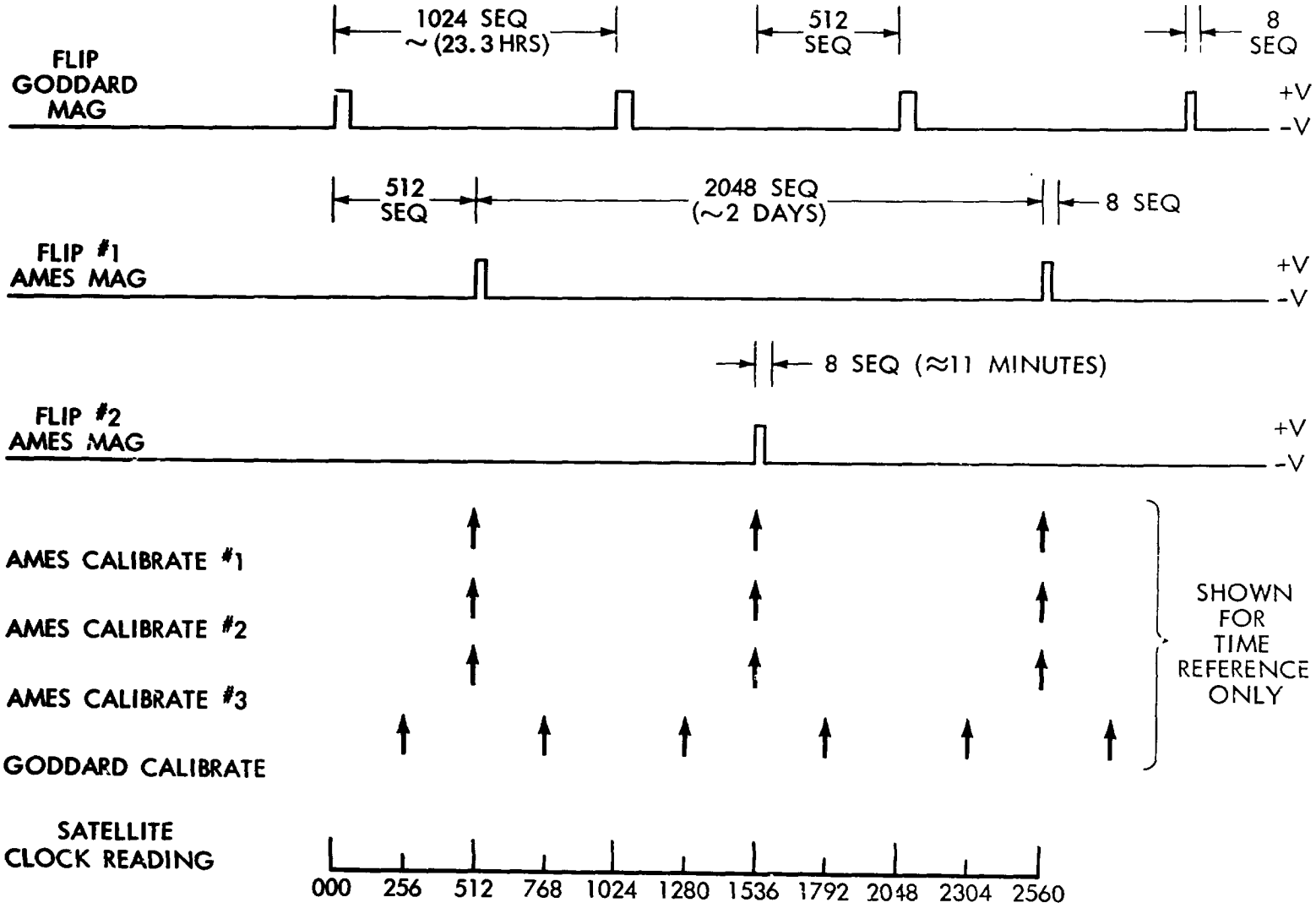
7. "Flip Goddard Magnetometer"

8. "Flip #1 Ames Magnetometer"

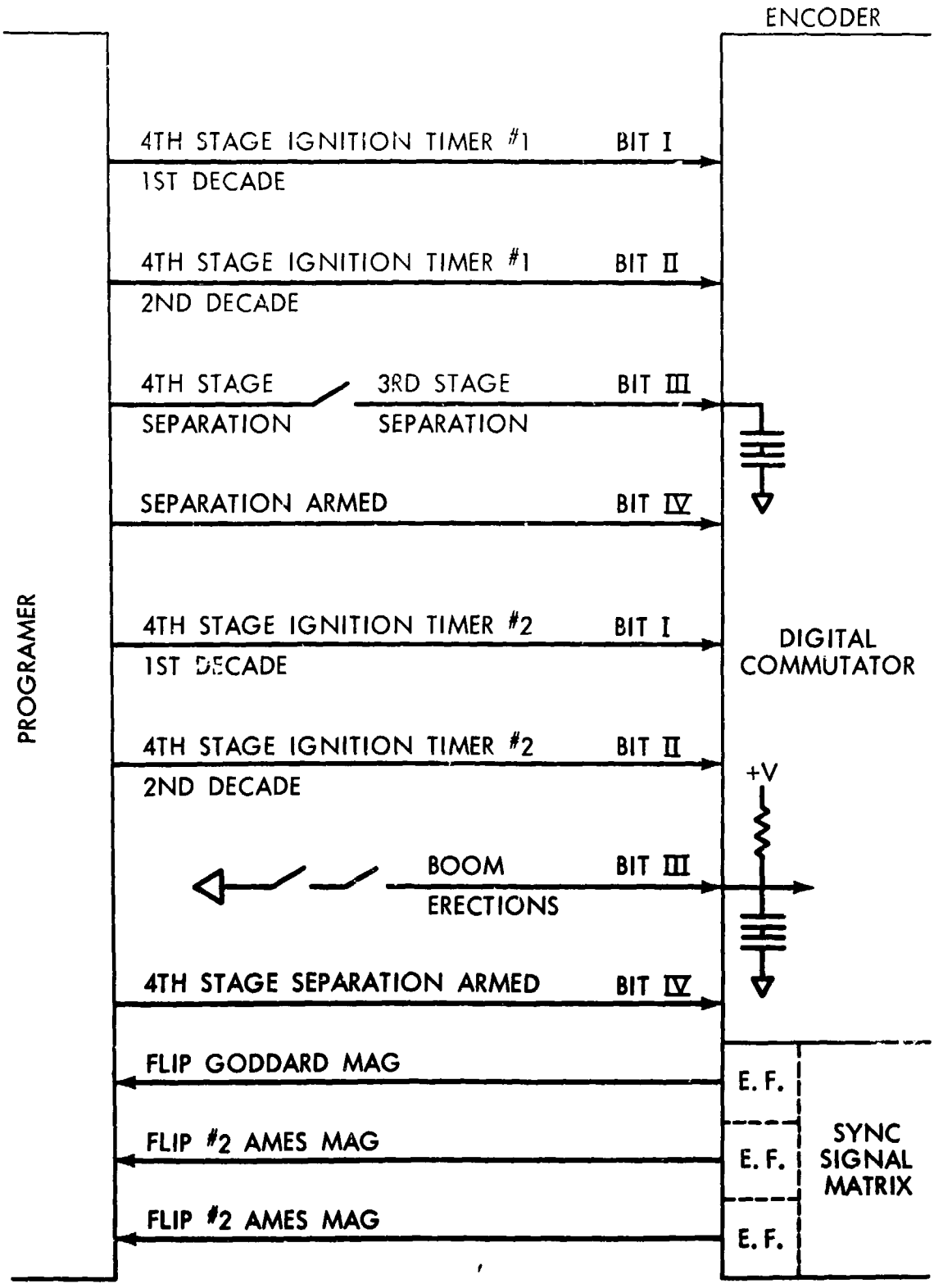
9. "Flip #2 Ames Magnetometer"

An attempt will be made to filter out short duration noise spikes from lines 7, 8 and 9.

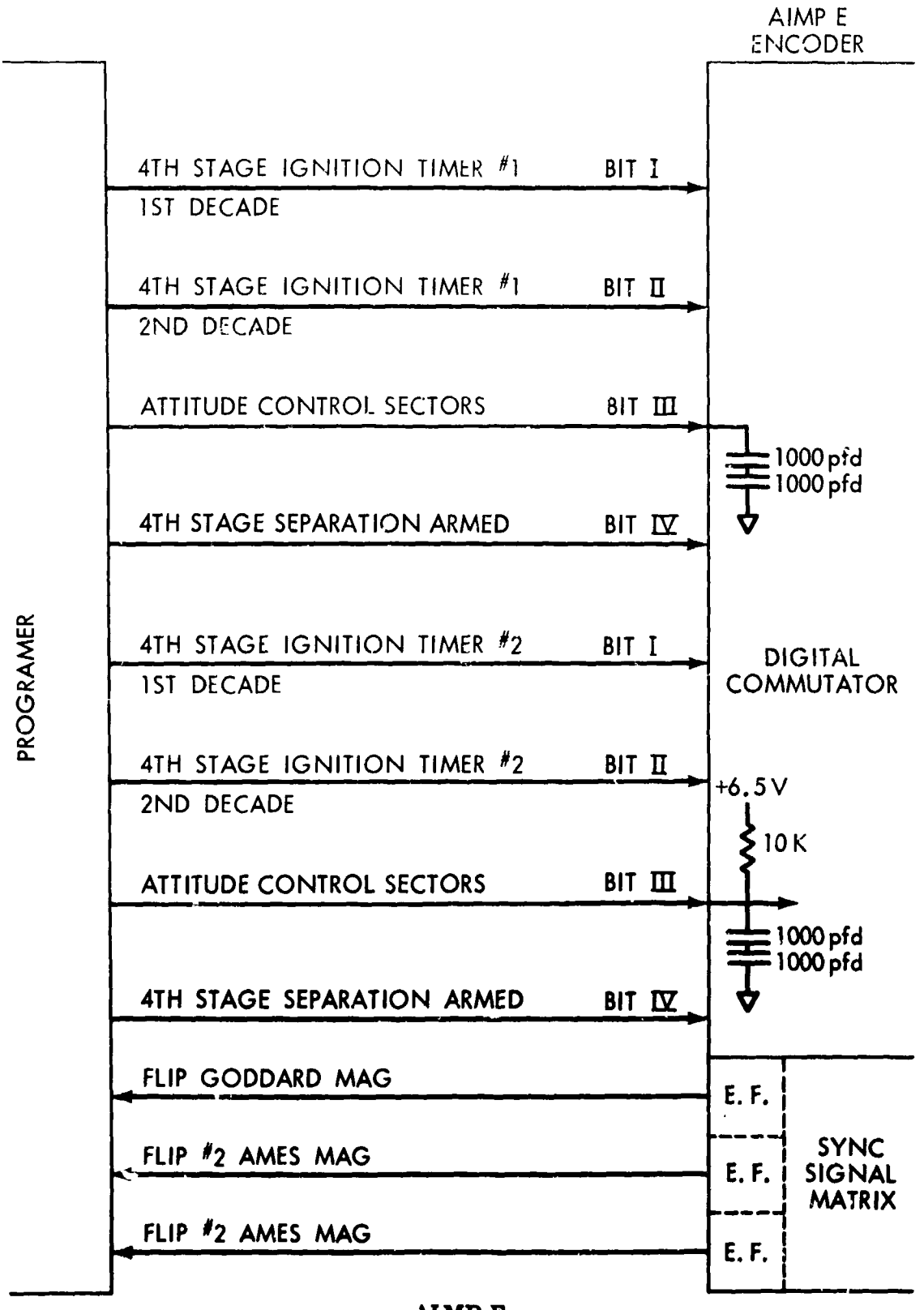
10. 3rd and 4th stage separation (first burst, Bit III) will be detected from a dropping resistor connected to the switched +12 V of the programmer card, timer section. (For AIMP D only)



Programmer Waveforms



IMP D
Interface with Programmer Functions



AIMP E
Interface with Programmer Functions

ADDITIONAL INTERFACE WITH PROGRAMMER CARDS FOR AIMP E

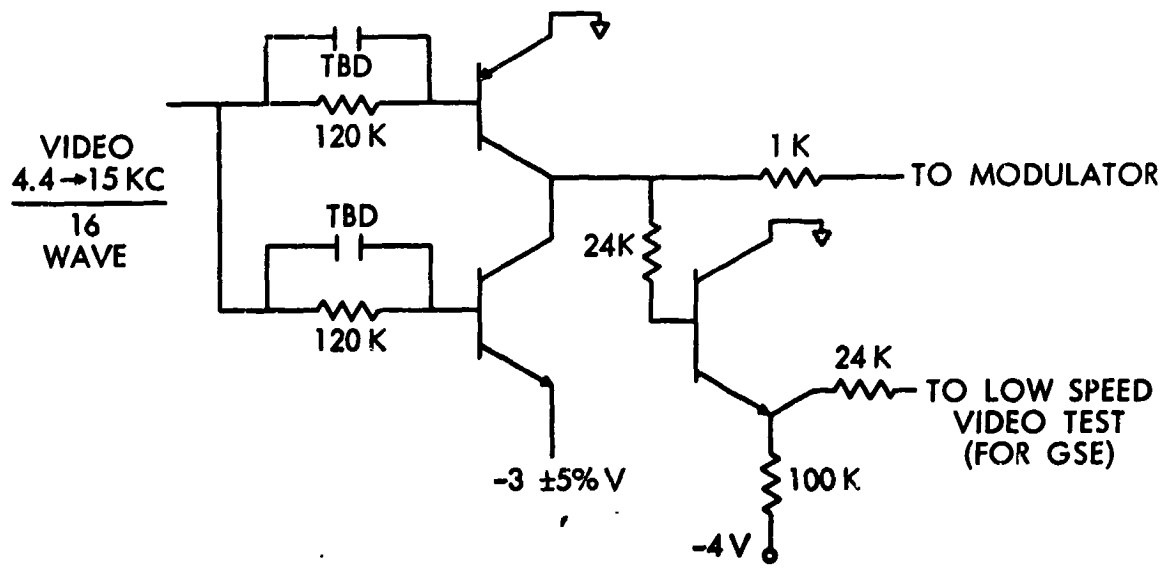
1. Attitude control sector indicator (first burst, bit III) - A voltage more positive than 3 volts into a 20 K ohm, 500 pfd encoder impedance will represent the "I" state. A voltage more negative than +0.5 volts into 44 K ohm, 500 pfd to ground will represent a logic "O".

2. Attitude control sector indicator (second burst, bit III) - A voltage more positive than 3 volts into a 20 K ohm, 500 pfd encoder impedance to ground and 10 K ohm impedance to +6.5 volts within the encoder will represent the "I" state. A voltage more negative than +0.5 volts into a 44 K ohm 500 pfd to ground and 10 K ohm to +6.5 volts encoder impedance will represent a logic "O".

INTERFACE WITH TRANSMITTER

The output to the transmitter is a complementary inverter with a 1 K ohm series impedance. The signal will be a series of unsymmetric square-wave bursts varying from ground to -3 volts (±5%) in which the unsymmetry produces an average of -1.5 volts over a period of 40 milliseconds. That is, the duty cycle of the pulses varies from greater than 50% to less than 50% for equal periods of time and equal amounts within the 40 millisecond periods of digital data. The analog data will be symmetric at all times.

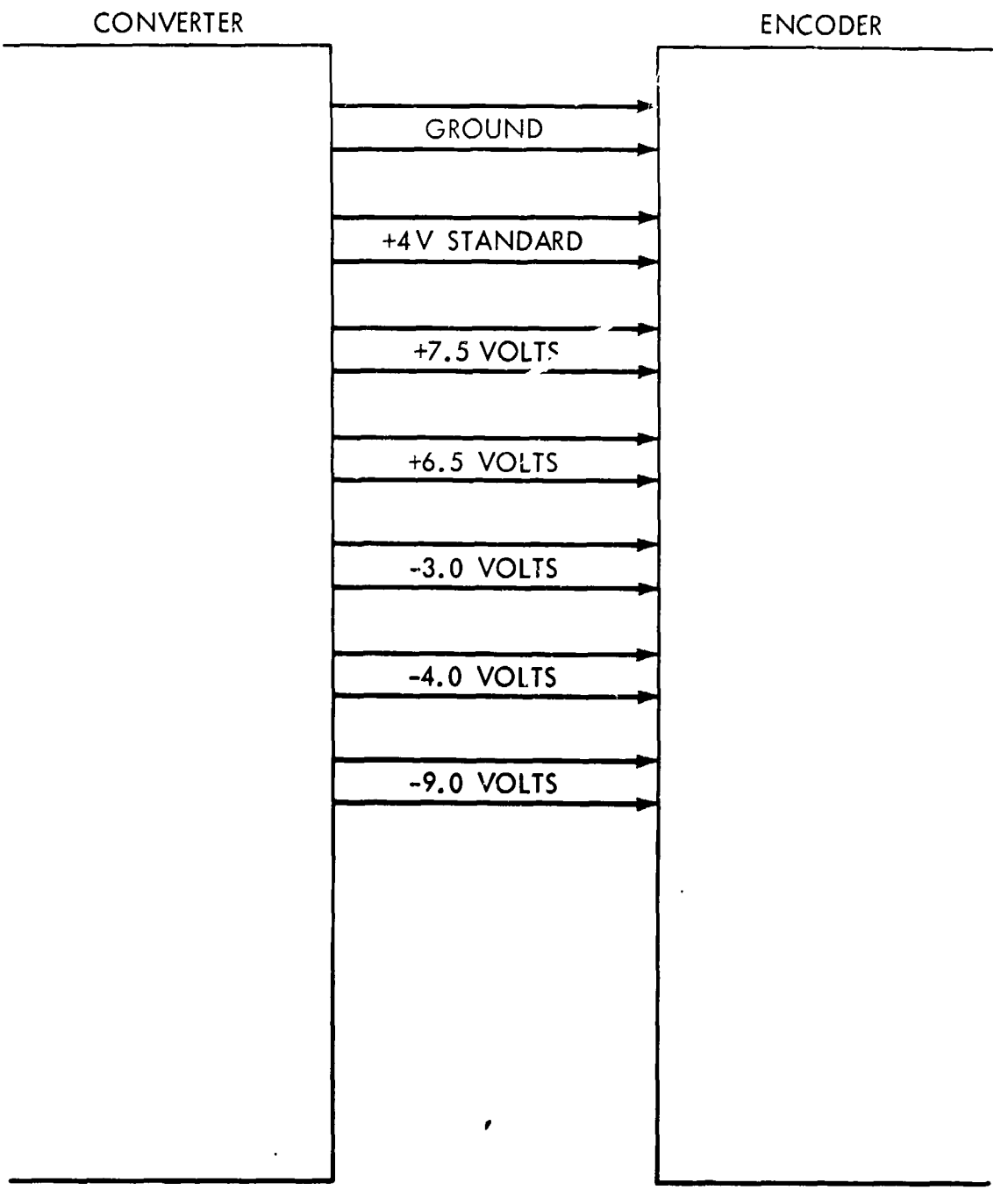
A 24 kilohm resistor isolates the "low speed video test" output from the modulator input. The minimum expected frequency is $\frac{4.4}{16}$ KC ≈270 cycles and the maximum expected frequency is $\frac{15}{16}$ KC = 940 cycles. The square-wave will have rise and fall times less than 5 microseconds, and "noise" spikes less than 1% of video signal.



Transmitter Interface Circuit

INTERFACE WITH ENCODER CONVERTER PACKAGE

1. The encoder converter package will contain the electronics for providing 5 voltages to the encoder electronics and will also house a voltage standard used for analog oscillator calibration. The estimated requirements for the encoder voltages are shown in table form on the following page.



Nominal Voltage	+7.5 Volts	+6.5 Volts	-3 Volts	-1 Volts	-9 Volts	Total
Max. Peak Current **Min. Current** **Average Current**	4.6 ma 2.2 ma 3.3 ma	65 ma 55 ma 60 ma	10.2 ma 1.4 ma 2.8 ma	55 ma 53 ma 54 ma	0.8 ma 0.6 ma 0.7 ma	
Max. Peak Power **Min. Power Drain** **Average Power**	35.0 mw 16.0 mw 25.0 mw	420 mw 355 mw 390 mw	30.6 mw 4.2 mw 8.4 mw	221 mw 215 mw 218 mw	7.2 mw 5.7 mw 5.9 mw	714 mw 596 mw 647 mw
Absolute Voltage Limits from Nominal at Average Current Level						
A. +40° C to +60° C **B. 0° C to +40° C** **C. -10° C to 0° C** **D. -30° C to -10° C**	±1.00% ±0.25% ±0.50% ±1.00%	±5% ±1% ±5% ±5%	±5% ±1% ±5% ±5%	±5% ±5% ±5% ±5%	±10% ±10% ±10% ±10%	
AC Impedance	Not critical	Low		Not critical		
Noise Spikes	Not critical	Low		Not critical		

Estimated Converter Requirements

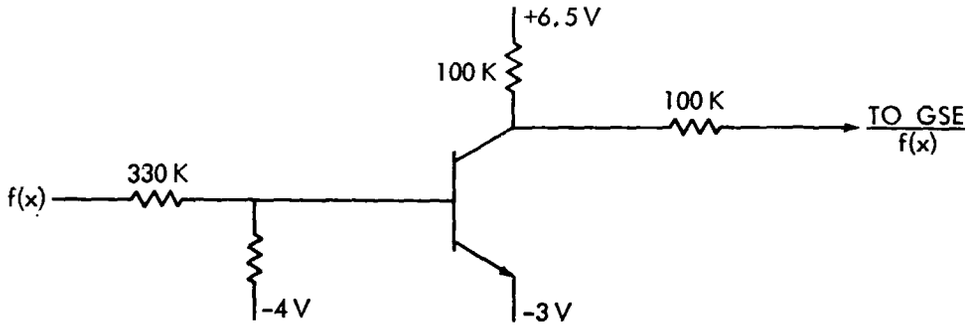
INTERFACE WITH ENCODER TEST FOR GSE FOR AIMP D

The following sync pulses will be provided for GSE.

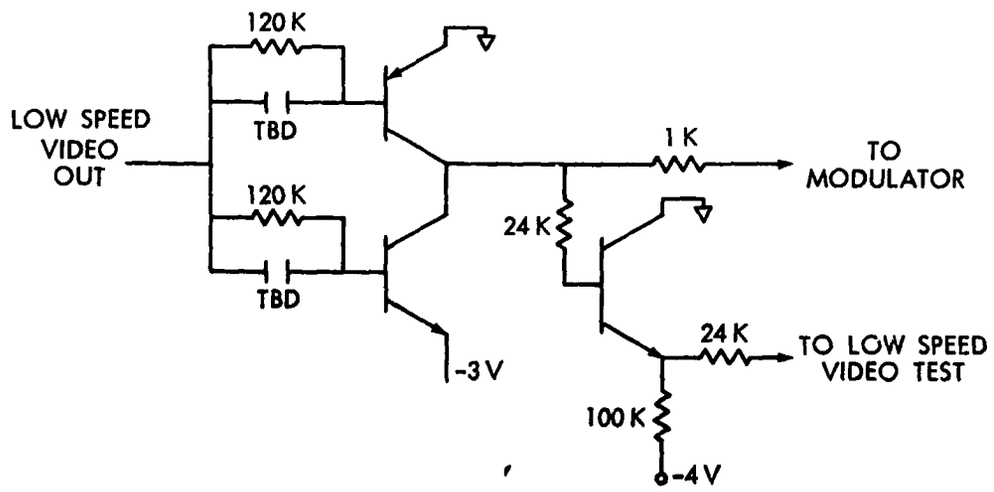
1. $\overline{2S}$ - negative at beginning of each burst
2. $\overline{A}$ - negative at beginning of each sequence
3. $\overline{a_2}$ - negative at beginning of "sequence one"
4. $\overline{C_8}$ - 800 cycle square wave

The following outputs will be provided.

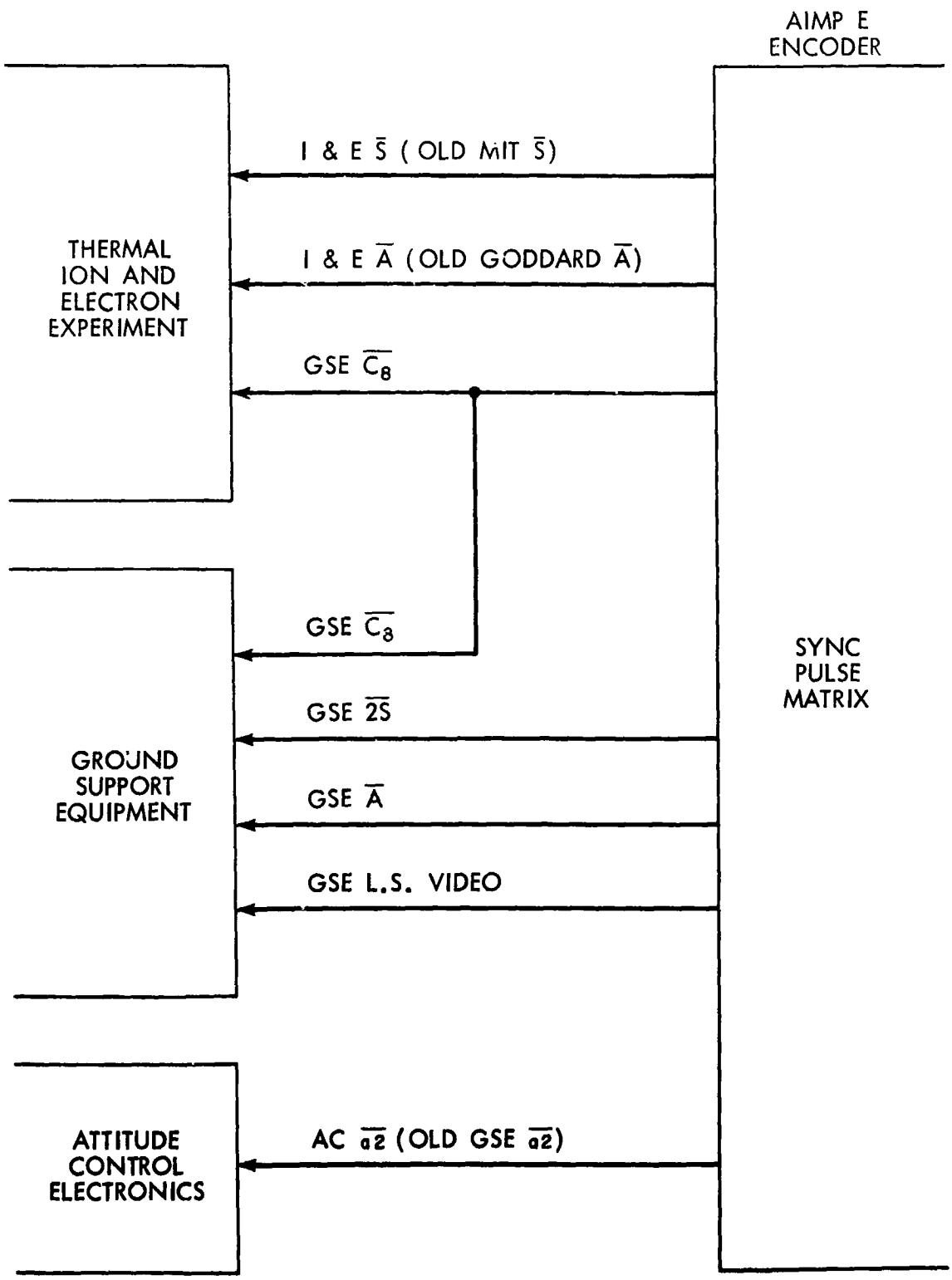
5. Low Speed Video Out (268 ⟶ 1000 cycles), an emitter follower with 24 K ohm output impedance isolated from the signal to transmitter.
6. High Speed Video Out (4.4 KC ⟶ 15 KC). To be used for DDP machine only (not to be used in T&E).



$\overline{f(x)} = \overline{2s}, \overline{A}, \overline{a_2}, \overline{C_8}$



Encoder Test Interface Circuit



AIMP E
I & E, Attitude Control & GSE Interface

INTERFACES WITH THERMAL ION AND ELECTRON
EXPERIMENT, ATTITUDE CONTROL, AND GSE FOR AIMP E

1. I & E $\overline{S}$ (old MIT $\overline{S}$) - 50/16 cps square wave, negative at the beginning of each channel (Encoder P_1 - pin 3).

2. I & E $\overline{A}$ (old Goddard $\overline{A}$) - negative for first half of every sequence, positive for second half of every sequence (Encoder P_3 - pin 1).

3. GSE $\overline{C_8}$ - 800 cycle square wave with unknown phase relationship to channel when loaded. Will be shared with ground support equipment and Thermal Ion Experiment.

4. GSE $\overline{2S}$ - negative at beginning of each burst.

5. GSE $\overline{A}$ - negative first half of sequence, positive second half of sequence.

6. AC $\overline{a_2}$ (old GSE $\overline{a_2}$) negative for sequences 1 and 2 positive sequences 3 and 4.

Each of these lines, 1 through 6, are 200 K ohm to +6.5 volts when positive and 100 K to -3 volts when negative.

7. GSE Low Speed Video same as on AIMP D.

8. GSE High Speed Video to be used for DDP machine only. Same as on AIMP D.

PART IV. DIGITAL DATA PROCESSOR (DDP) FOR IMP's D&E

A. GENERAL

The DDP has been incorporated into the encoding system to accept experiment pulses that must be either accumulated or stored until readout

The capacity is 188 bits that are readout every 40.96 seconds, 8 bits/channel. The 188 bits may be arranged in various combinations of accumulator lengths. In addition, two types of accumulators are available; one is called an "S" type and the other an "S-T" type accumulator.

The "S" type accumulator is a straight binary counter similar to those used in IMP's A, B & C while the "S-T" type accumulator is used for experiments that may cause an overflow of the accumulator. "S-T" stands for SIGNAL or TIME. The "S-T" type will accumulate until it overflows and will then count clock pulses for the rest of the accumulation period. Thus for low counting rates, the accumulator will readout the number of pulses counted and for high counting rates will give a measure of counting rate (e.g., the time required to overflow the accumulator).

The maximum rate any accumulator will accept is 500 KC but an effort will be made to tailor the speed versus power characteristics of the DDP. Thus, each experimenter is requested to give us the maximum possible rate his experiment will produce. We will build accumulators with maximum rates of 500 KC, 250 KC and 125 KC.

B. ACCUMULATOR GROUPINGS (SIZE)

As shown on the telemetry format (Section II-7), the basic accumulator word is 32 bits that are readout every 40.96 seconds (4 channels). Since an entire 32 bit accumulator is frozen for the 4 channel readout, the minimum "dead time" will be 1.28 seconds out of 40.96 seconds for a ratio of dead time to accumulation time of 1/32. Each 32 bit accumulator may be broken up into as many as 4 accumulators or as few as one accumulator where the number of bits in each accumulator is divisible by 2. In addition, "S" and "S-T" type accumulators may be combined into a 32 bit word. Some possible examples follow and they will be given:

5a = 16 bits "S-T" type
5b = 16 bits "S" type

or

1a = 20 bits "S" type
1b = 12 bits "S" type

Many more combinations are possible, an example of an impossible combination follows:

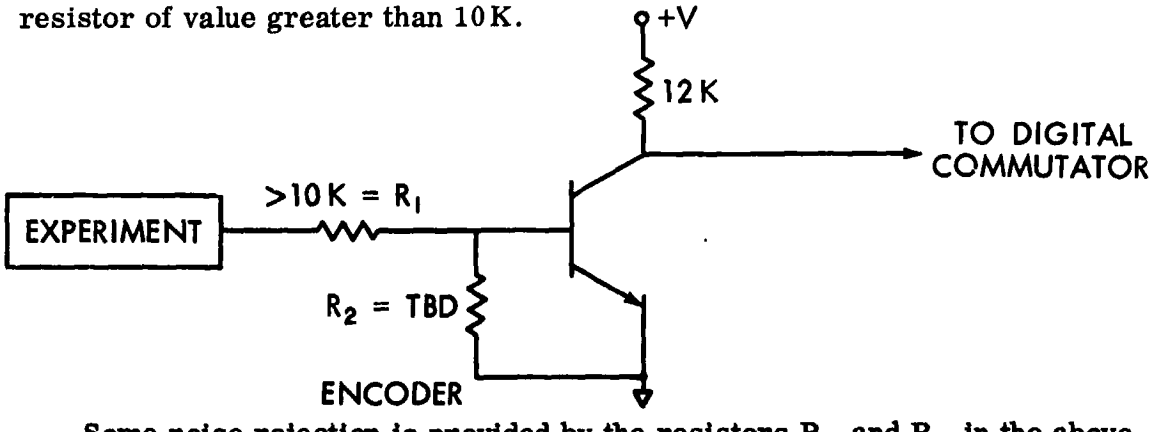
5a = 19 bits any type
5b = 13 bits any type

Accumulators not broken up into groups divisible by 4 will result in a single sexadecimal burst containing information from two different accumulators. Provisions must be made to take care of this during satellite checkout and bit reordering will be required during data processing. In addition, the least significant bit will be readout first as was done in IMP's A, B & C.

C. ACCUMULATOR INPUT CHARACTERISTICS

As previously mentioned, an attempt will be made to tailor the speed power characteristics of the accumulator. The maximum rate an accumulator will accept is a 500 KC sine wave or pulses with a duration of greater than one microsecond. Over-all system performance will be increased if the experimenter will inform the project staff as to his maximum possible input rates and minimum pulse duration.

The input impedance that will be seen by the experiment pulse will be a resistor of value greater than 10 K.



Some noise rejection is provided by the resistors R_1 and R_2 in the above figure. The input signal will be rejected when its amplitude is less than 2 V ±0.5 V depending on speed and temperature. This amplitude measured at the "in" terminal with the experiment connected. When the pulse is not present

the experiment output must be less than +0.5 V and when the pulse is present, the experiment output must be between +3.5 V and +7 V. Thus the accumulators will not accept negative going pulses and will get confused if a positive voltage is present during standby operation.

In order to solve any interface problems that may occur, a simulator will be sent to the experimenter, at his request, after the design freeze date. This simulator will contain the accumulator signal conditioner and the first four bits of his accumulator.

D. FREEZE

This is not really an electrical interface since the experimenter has no control over it. However, an understanding of freeze may be useful to the experimenter in interpreting his data.

The word freeze means, "will not accept pulses". Accumulators are always frozen during readout so that they will not change during the accumulator readout. Every 32 bit word will be frozen for the four channels during which it is readout. It is realized that this results in a dead time (1/16) that is undesirable, but the circuitry required to freeze is very simple compared to a rapid transfer and hold in buffer storage scheme. Again, note that freeze may be made longer if experimenters time-share adjacent accumulators.

E. RESET

Each 32 bit group of accumulators has two options for reset:

1. The entire 32 bits are reset after readout (at end of freeze).

2. None of the 32 bits are reset after readout (at end of freeze).

"S" type accumulators are reset to all 1's (highest number). The first pulse received from the experiment will then flip the entire accumulator to its "0" state. From then on it will count normally. Thus, the information telemetered from the resetable "S" type accumulators will indicate one less count than was actually received (e.g., if the accumulator reads 29,986 counts, then 29,987 counts were actually received).

"S-T" type accumulators are essentially reset to zero as far as the experimenter is concerned. Thus, if the accumulator reads 29,986 counts,

then 29,986 counts were received. The state of the most significant bit will tell whether these counts were from the experiment or from the encoder clock.

F. "S-T" TYPE ACCUMULATOR

This type accumulator will count signal pulses (S) up to a maximum number and will then count clock pulses (T) for the rest of the accumulation period. Thus, either signal counts (S) or counting rate (T) will be telemetered. The purpose of the device is to take care of overflow, thus increasing the dynamic range. It should be noted that the accumulation period and the clock pulses are slaves to the same 409.6 KC satellite Xtal.

Although "S-T" accumulators may be made of any size following the rules in paragraph B, a description will be given for a 16 bit "S-T" accumulator. If a different size accumulator is required, the principal of operation is the same but the clock pulse frequency will be changed so as not to overflow in the count (T) mode.

Referring to figure IV-1, the 16 bit "S-T" accumulator works as follows:

1. After readout (freeze), the entire 32 bit word, of which the 16 bit "S-T" accumulator is part, is reset to all 1's and allows the 800 CPS clock through.

2. The first clock pulse will come through within 2.5 MS and flip all 12 accumulators to zero and allow the signal "S" input to come through.

3. The accumulator will allow signal pulses (S) through from the experiment until the 16th bit again changes to "1". This will take exactly 32,768 pulses, at which time the 800 CPS clock (T) will count until the accumulator is again frozen for readout.

4. At a 800 CPS clock rate, the accumulator will acquire 800 x 39.68 = 31,744 pulses in the maximum accumulation time of 36.224 seconds. Since it would take 1,024 clock pulses to overflow in the T mode, an 11% safety factor exists.

Readout

If the 16th bit of the accumulator is "0", then the readout is the number of pulses acquired in the 39.68 second accumulation period. Note that it is unnecessary to add the "1" to the count.

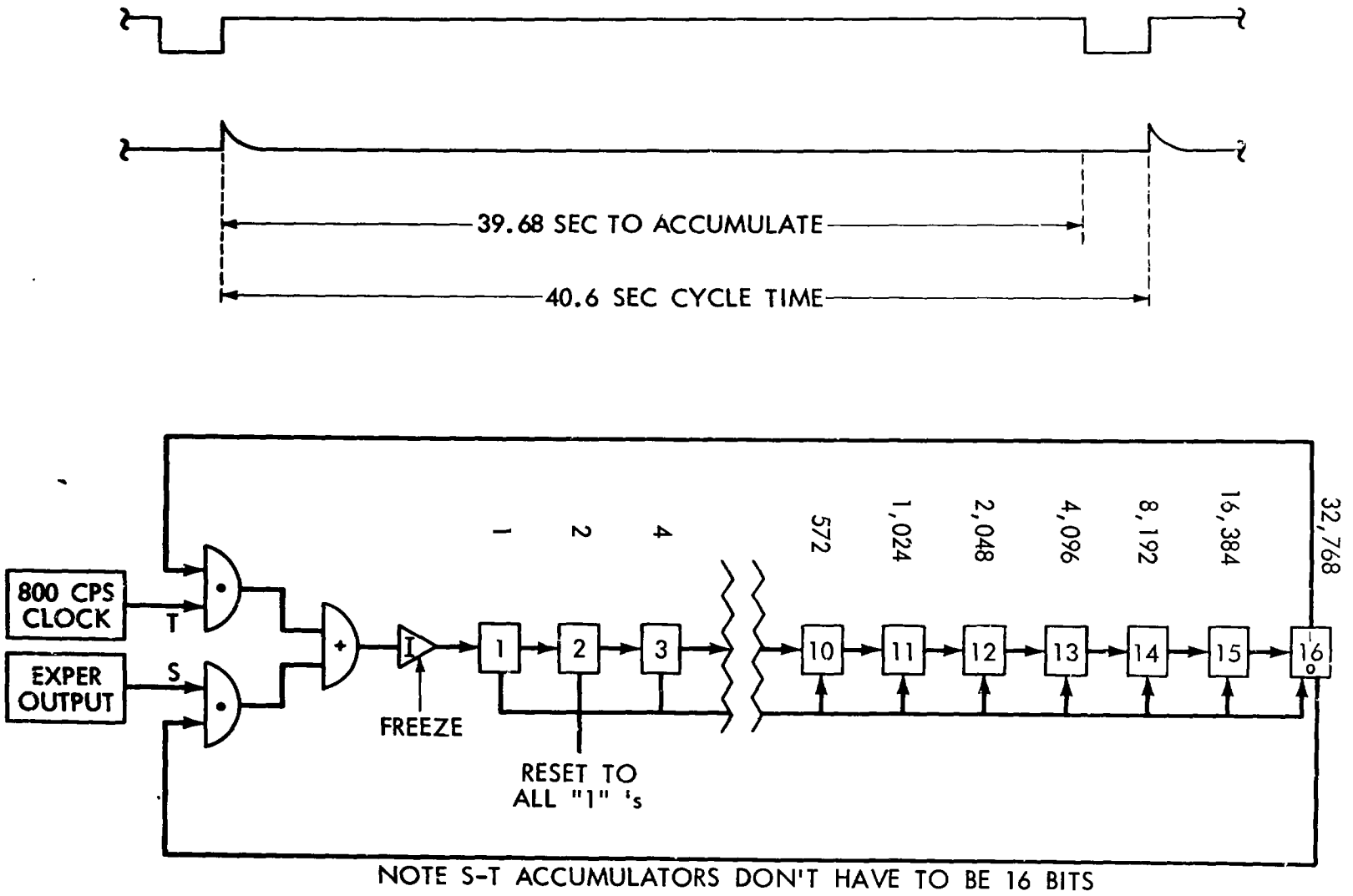


Figure IV-1. "S-T" Accumulator (16 Bit)

If the 16th bit of the accumulator is "1", the first 15 bits of the accumulator give the number of clock pulses acquired after the accumulator overflowed to a resolution of about 1.25 MS.

Assuming an Xtal accuracy of exactly 409.6 KC, thus a sequence time of exactly 81.92 seconds the counting rate will be:

$$\text{Counting Rate} = \frac{32{,}768}{(39.68 - .00125 \times \text{T count}) \pm .00125} \text{ in pulses/second}$$

Since the Xtal accuracy is only 0.2% although its stability is better than .01% and since, if it shatters, the clock will no longer be Xtal controlled, the above equation might be written in terms of the actual sequence rate. The ratio of the clock frequency to the accumulation period will remain constant in the event of an Xtal failure so it probably isn't necessary to take sequence rate into account in the equation.

In the "S" mode, however, actual sequence rate is important.